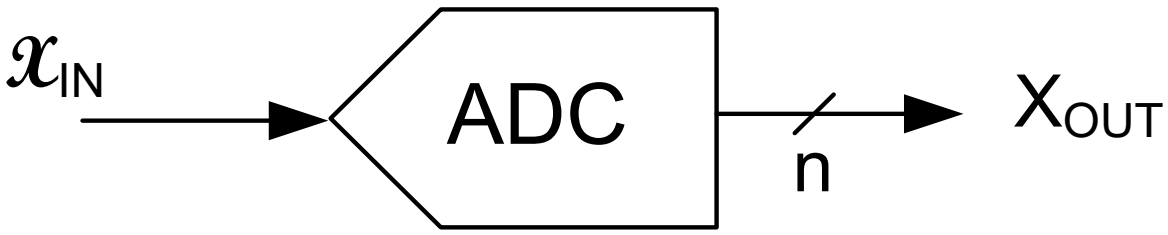
EE 435

Lecture 38

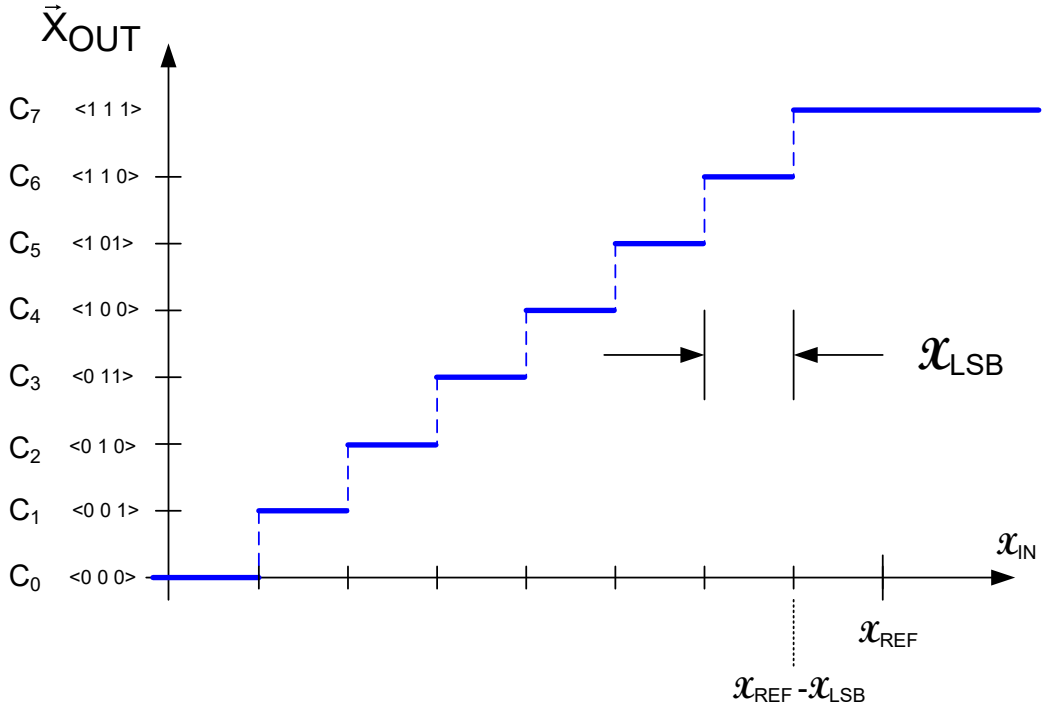
ADC Design

Analog to Digital Converters



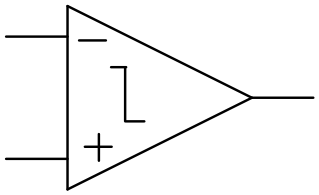
Will now focus on design of ADCs

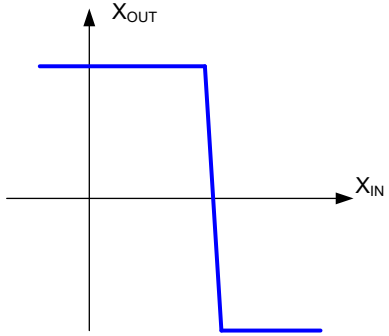
Analog to Digital Converters



Analog to Digital Converters

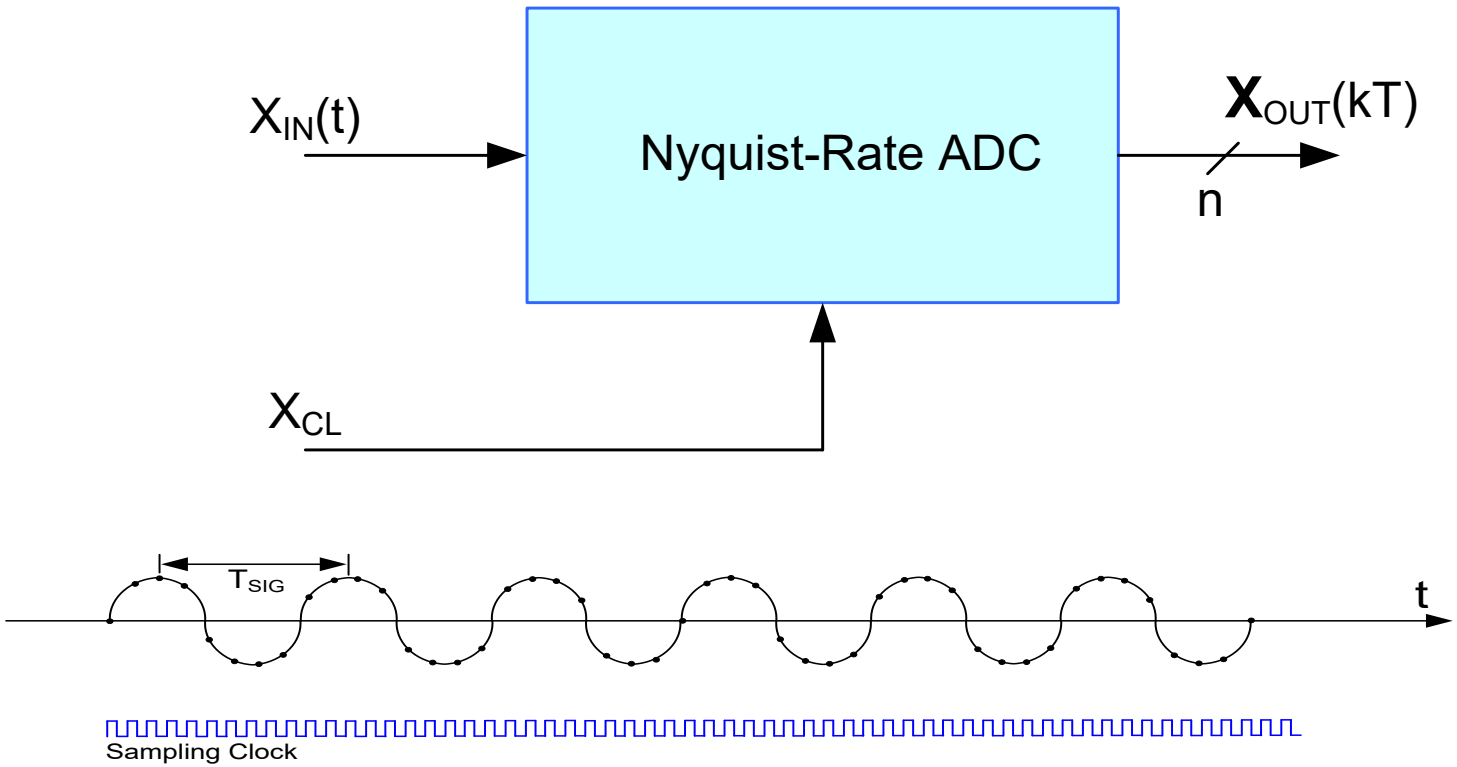
The conversion from analog to digital in most ADCs is done with comparators





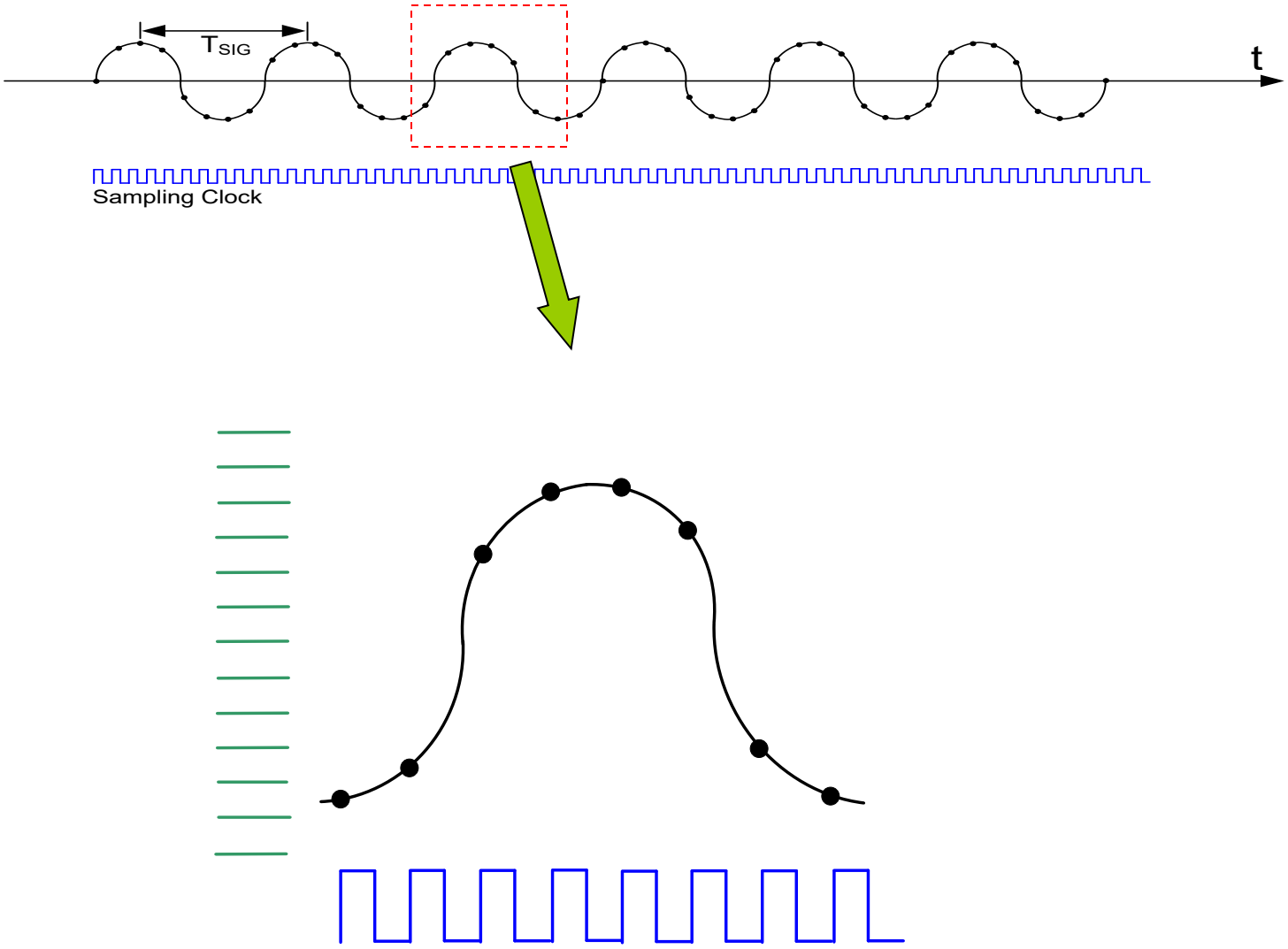
Most ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

Nyquist Rate

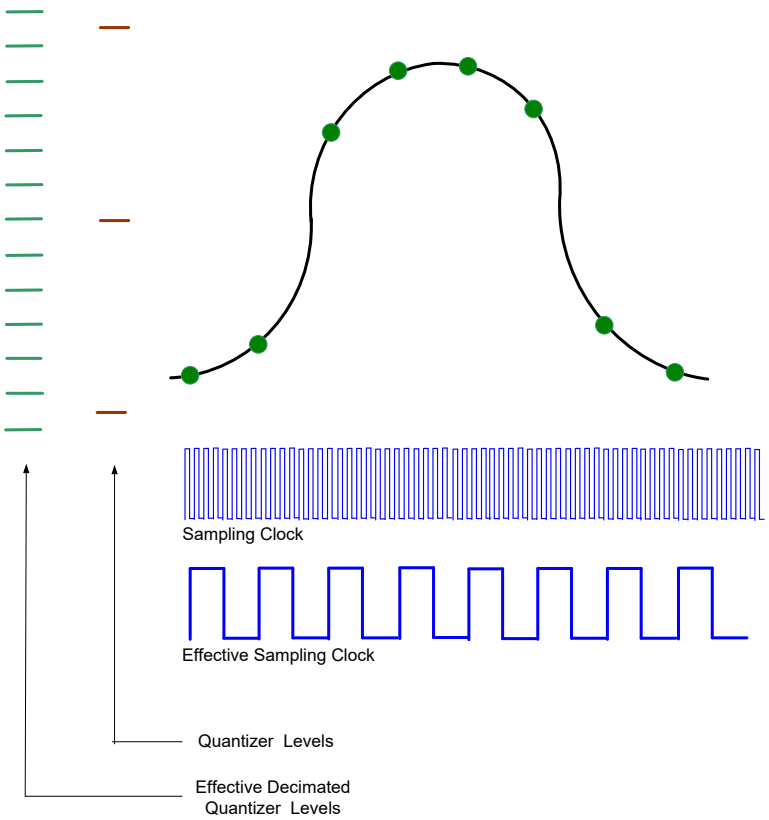


Nyquist Rate Data Converters provide one output for each period of the sampling clock

Nyquist Rate



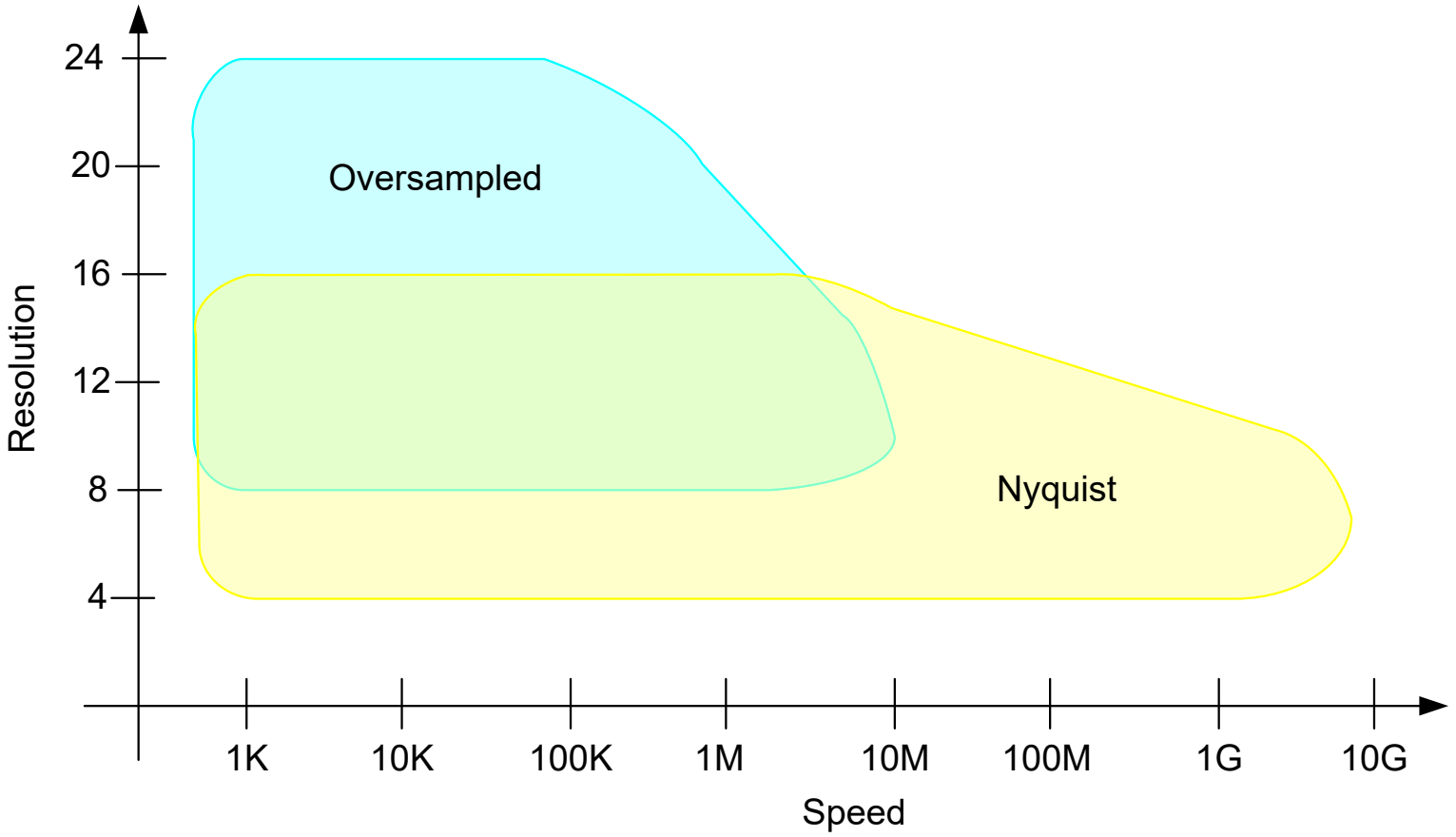
Over-Sampled



Over-Sampled Data Converters require multiple sampling clock periods for each output

Over-sampling ratios of 128:1 or 64:1 are common
Dramatic reduction in quantization noise effects
Limited to relatively low effective conversion rates

Data Converter Type Chart



ADC Types

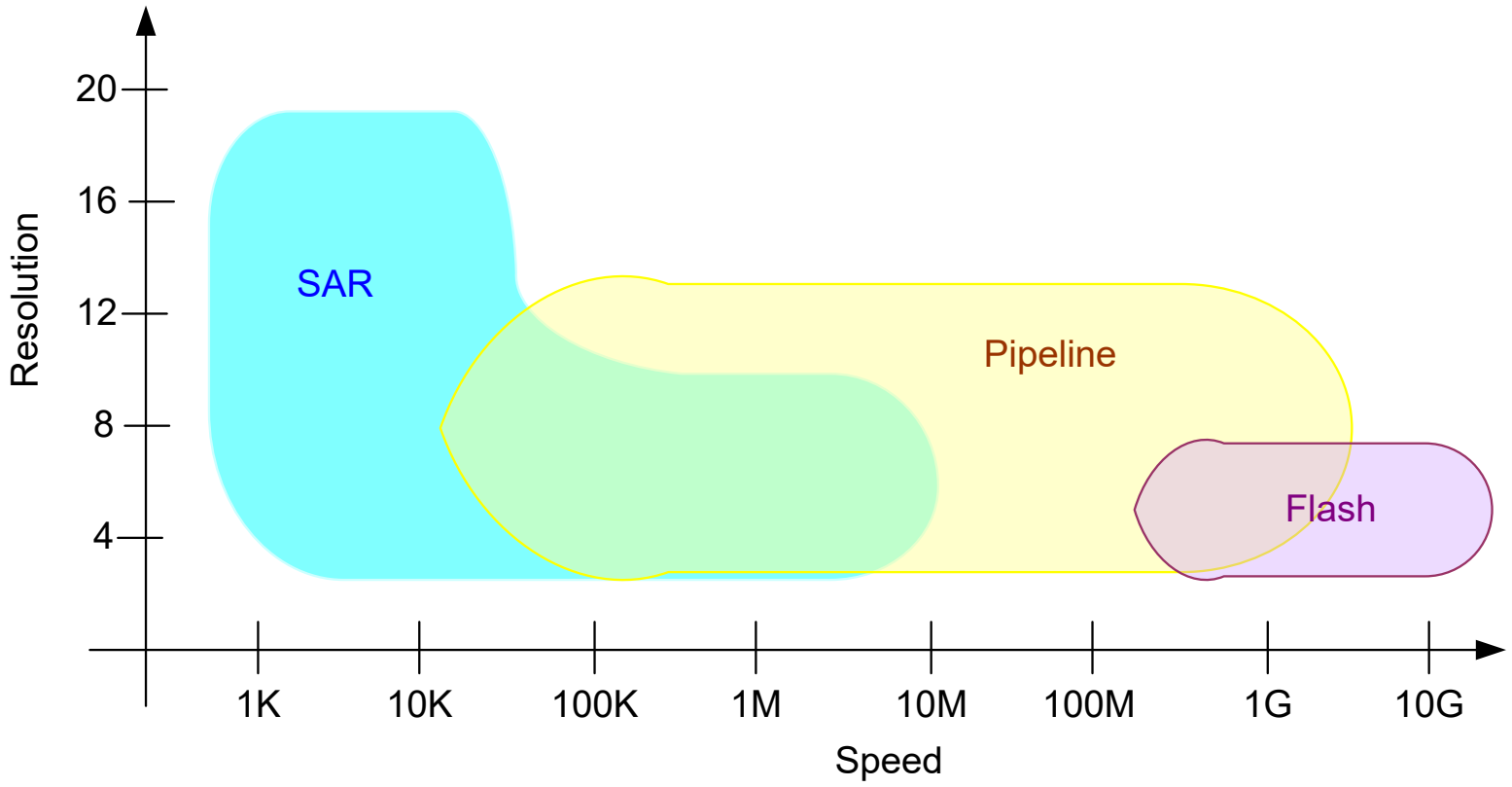
Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Nyqyist Rate Usage Structures



What Architectures are Actually Used

DACs
Texas Instruments Mar 1, 2023

String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

ADCs
Texas Instruments April 13 2023

SAR	728
Pipeline	294
Delta Sigma	187
Folding Interpolating	66
Delta Sigma Modulator	9
Two-Step	6
Flash	3
Total	1293

- These are catalog parts
- Specific details about architecture usually absent in data sheets
- Some (many) in list are slight variants and carry different part numbers
- Variety of converters used in ASIC applications will be larger

ADC Types

Nyquist Rate

- Flash
- Pipeline
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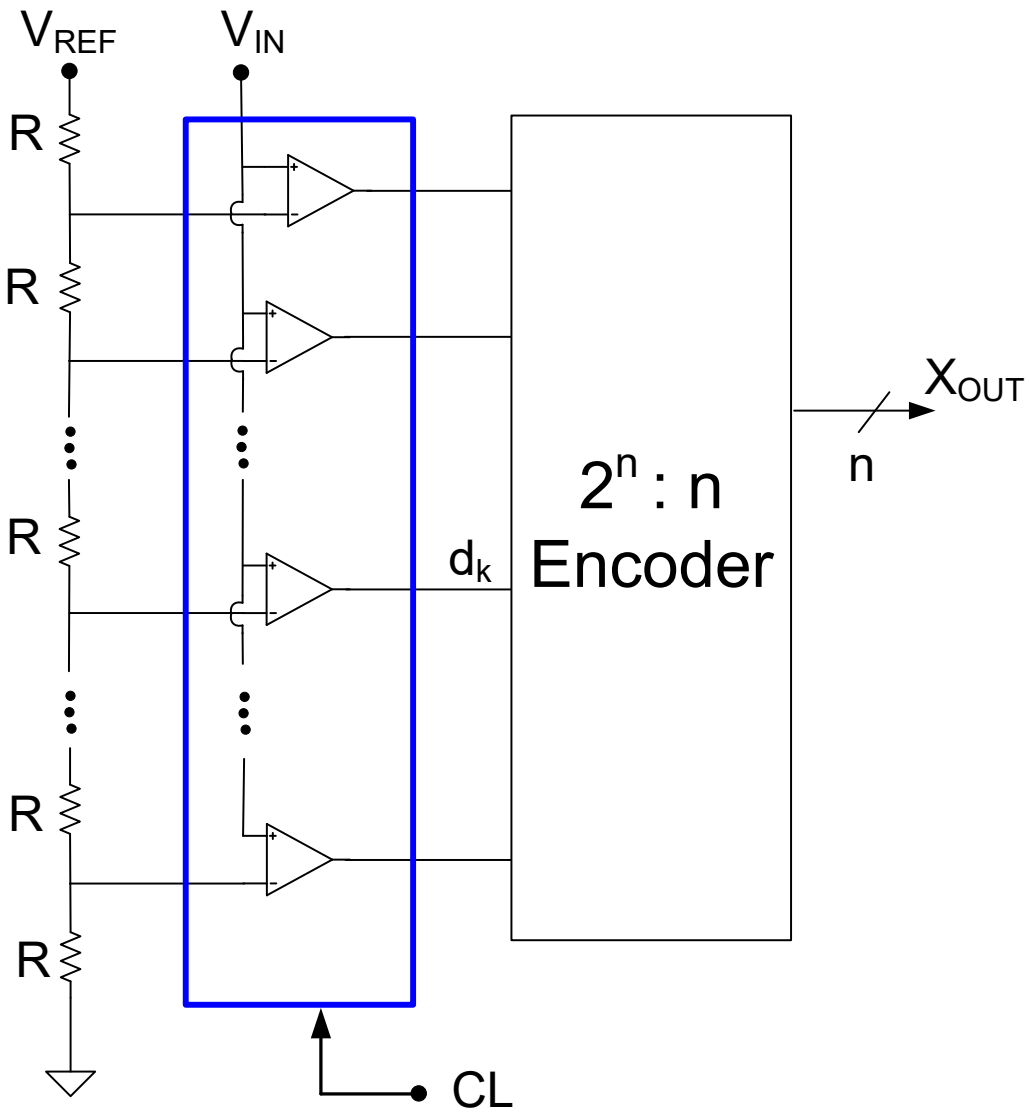
Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

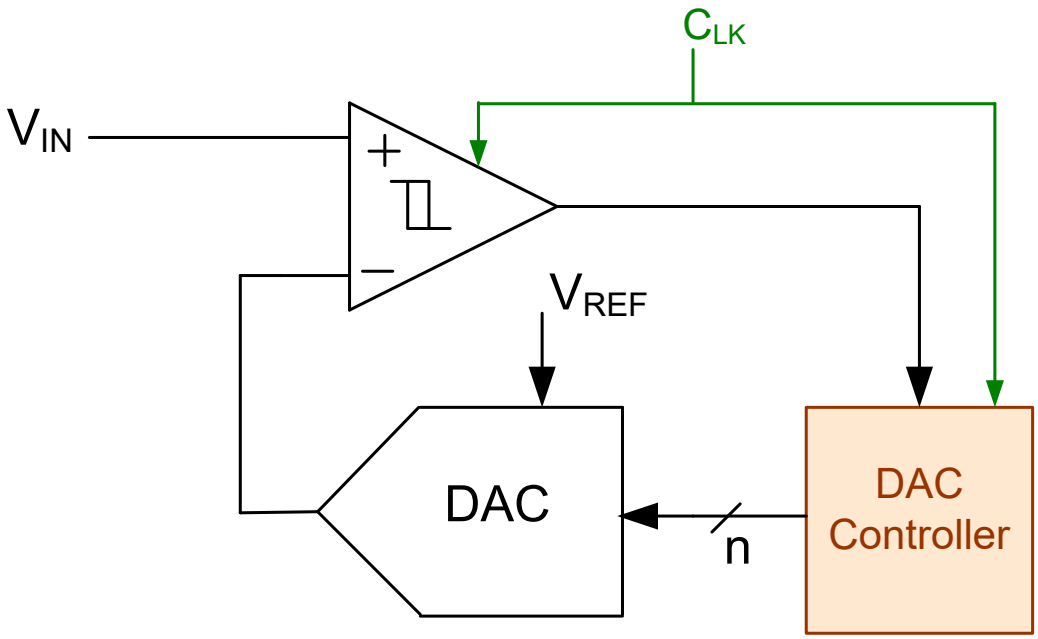
All have comparable conversion rates

Basic approach in all is very similar

Flash ADC

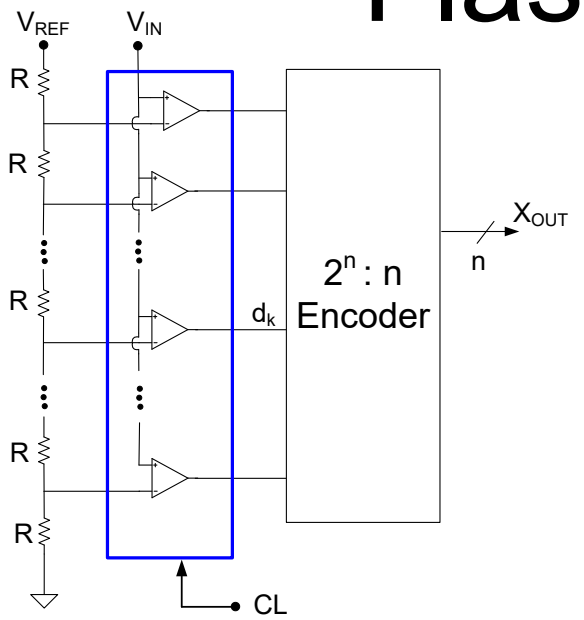


SAR ADC



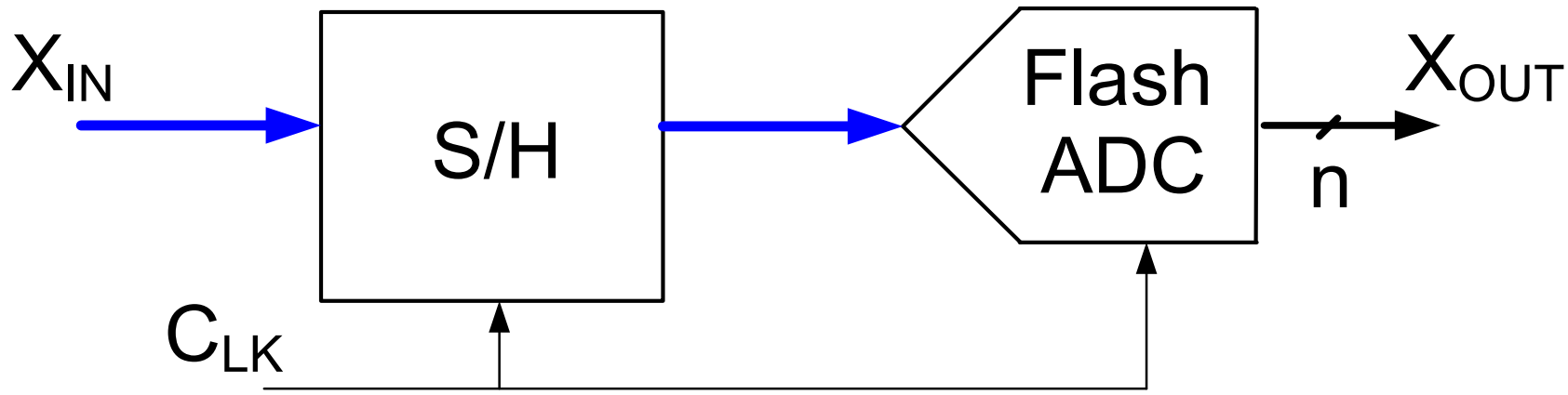
- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small

Flash ADC



Asynchronous operation (benefit or liability?)
Vulnerable to missing codes
High number of comparators needed (for large n)
R-string area requires considerable area and source of INL limitations
Offset voltage of comparators of concern
Simultaneous switching of large number of comparators can cause supply glitches
Large parasitic capacitance on V_{IN} pin
Bubbles in output can occur
Metastability an issue
Power dissipation can be large

Flash ADC with Front-End S/H



Prevents input to ADC from changing during sampling (Synchronous instead of Asynchronous)

Performance of ADC can be no better than that of the S/H

Significant amount of effort and power may go into the S/H

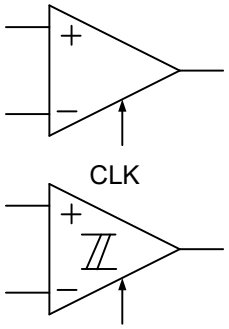
Comparators

High-Gain Saturating Amplifier

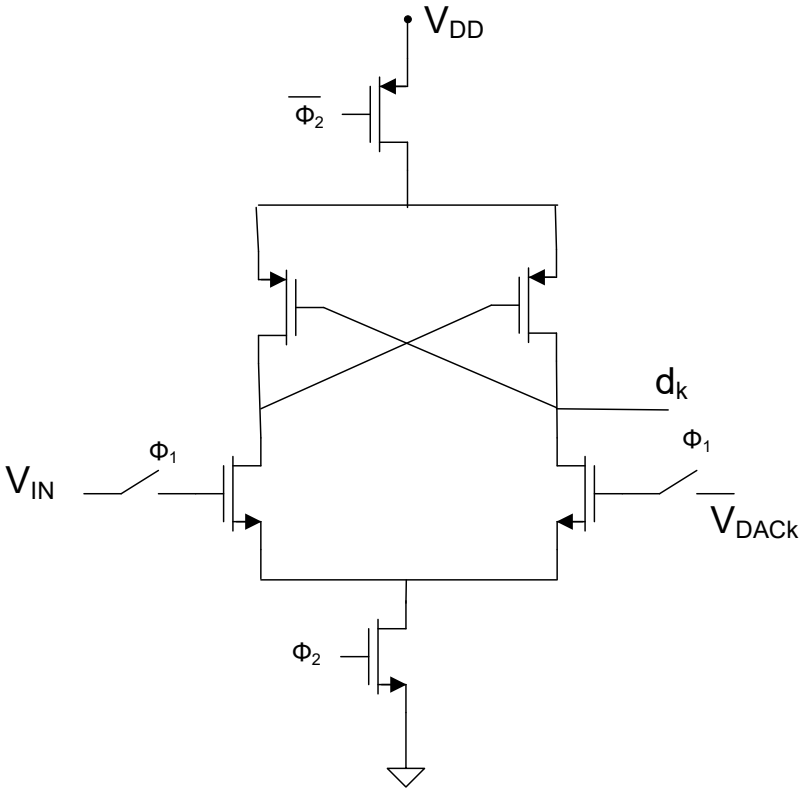
Clocked Comparator

Linear High-gain Amplifier

Regenerative Feedback Amplifier

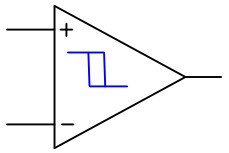


Clocked Comparator

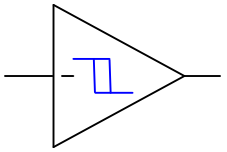


Regenerative Feedback

Regenerative Comparators



Differential



Single-Ended

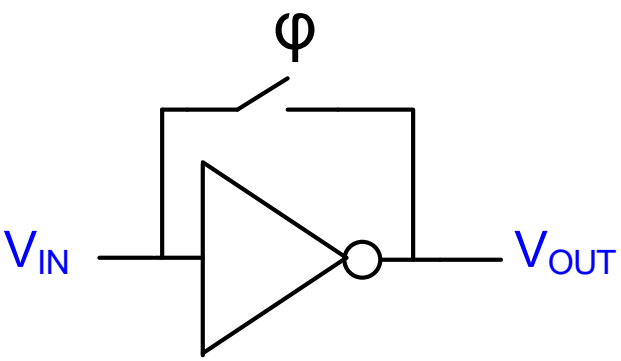
Large offset voltage (100mV or more)

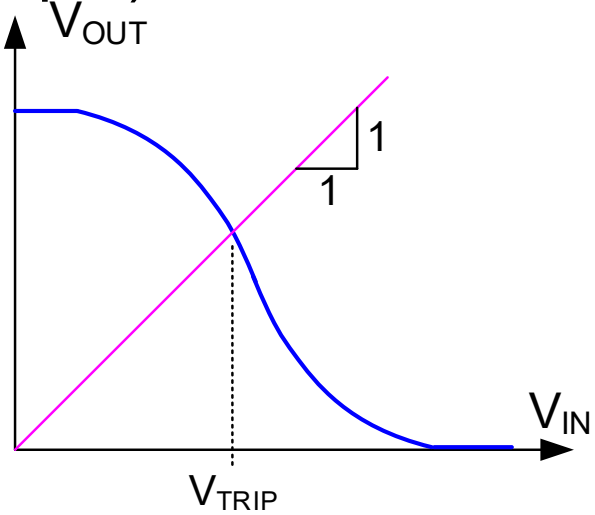
Previous-decision affects offset

Clocked Comparator

(Single-ended input)

Recall:





Forcing $V_{OUT}=V_{IN}$ (by closing switch φ) forces the amplifier to operate at the trip point

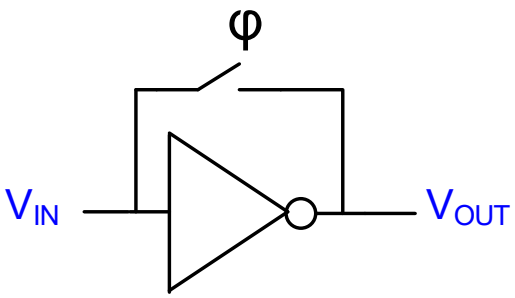
Concept applicable irrespective of how large the gain of the amplifier is

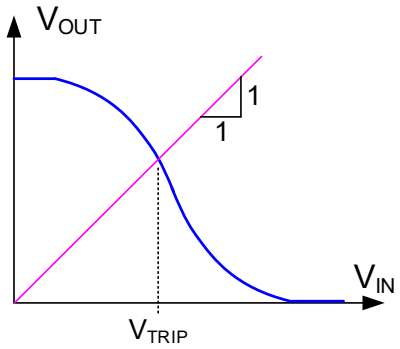
But power dissipation may be high when φ is activated

How can this property be exploited to form clocked comparator?

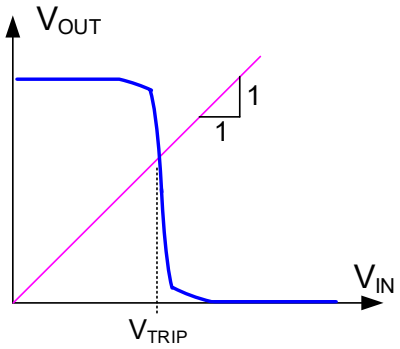
Clocked Comparator

(Single-ended input)

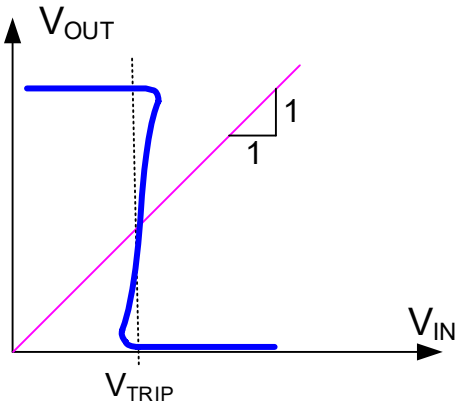




Low Gain Comparator



High Gain Comparator



High Gain Comparator with hysteresis (regenerative)

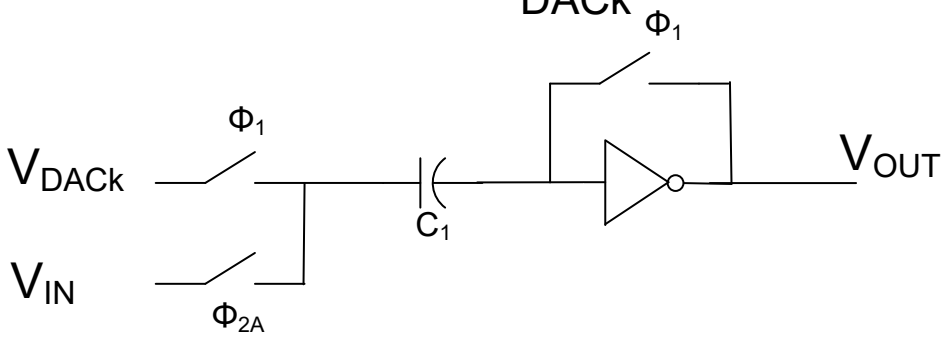
If goal is to compare V_{IN} with V_{TRIP}, have clocked comparator

But comparison point highly process dependent thus limiting this approach

Clocked Comparator

(Single-ended input)

Comparison now with V_{DACk}

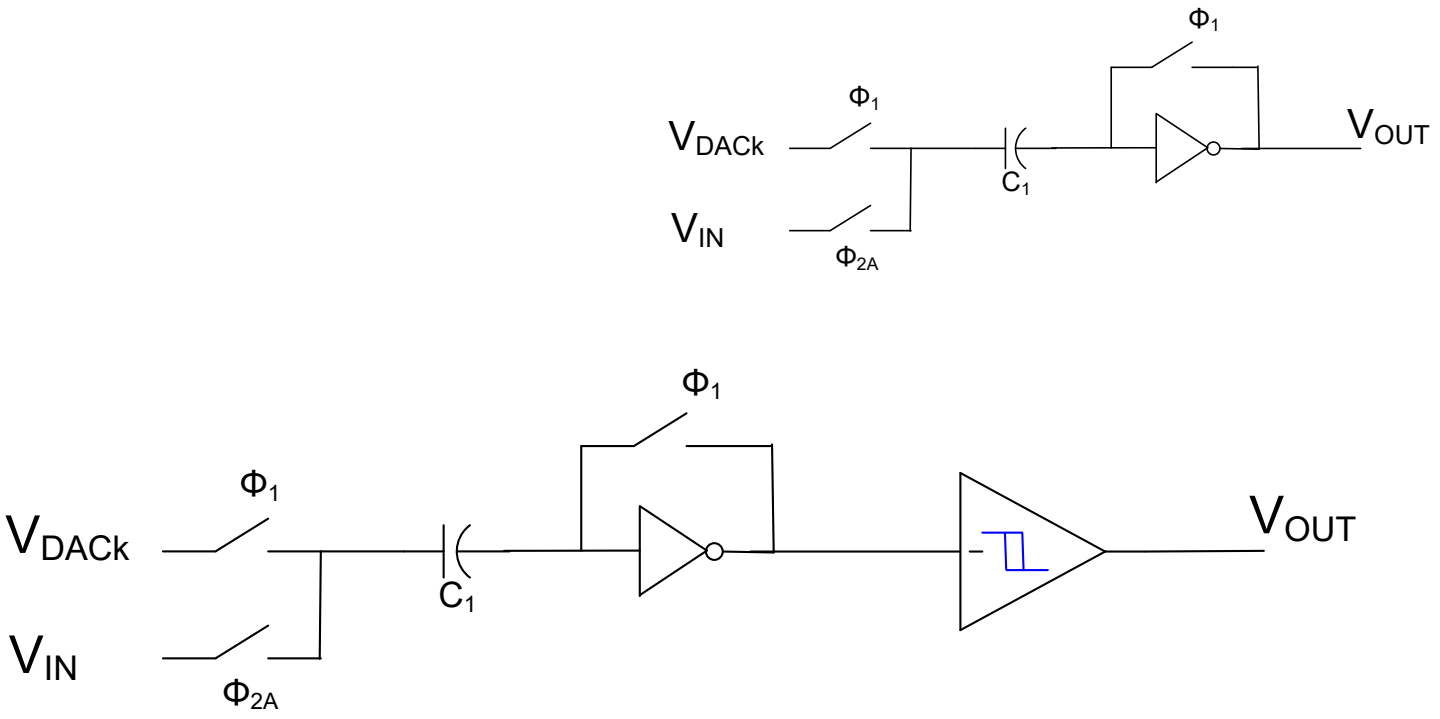


Amplifier may be viewed as a preamplifier with offset compensation

- Ideally removes all offset effects
- May not have a large enough gain
- Regenerative latch often used (either for gain block or following)

Clocked Comparator

(Single-ended input)

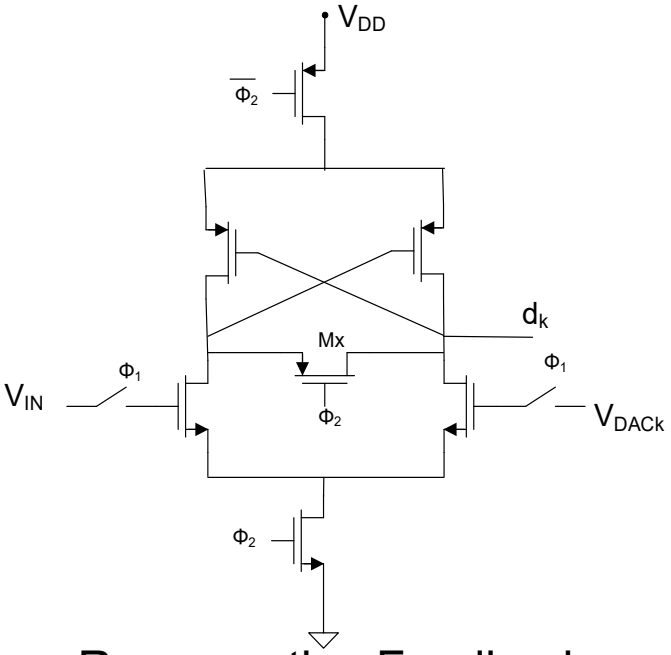


Preamplifier with offset compensation and regenerative latch

Gain of preamplifier may still not be large enough

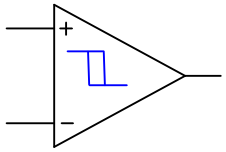
Can use two pre-amp stages and/or offset compensation on latch

Clocked Comparator with Regenerative Feedback

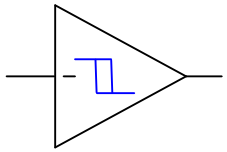


Regenerative Feedback

Regenerative Comparators



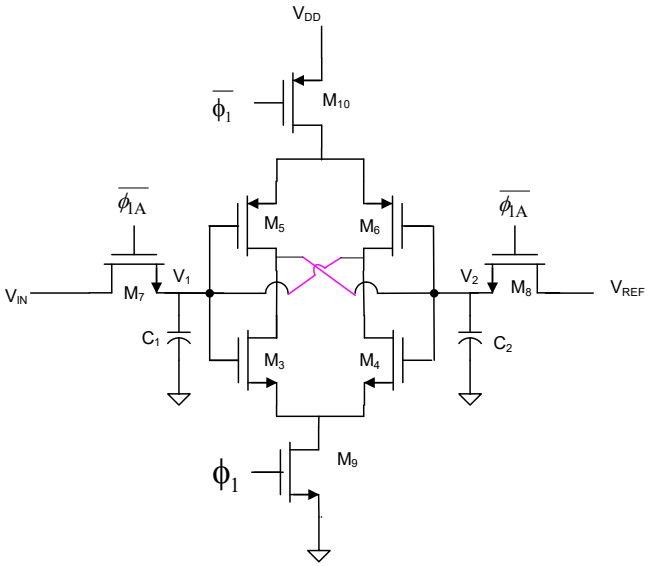
Differential

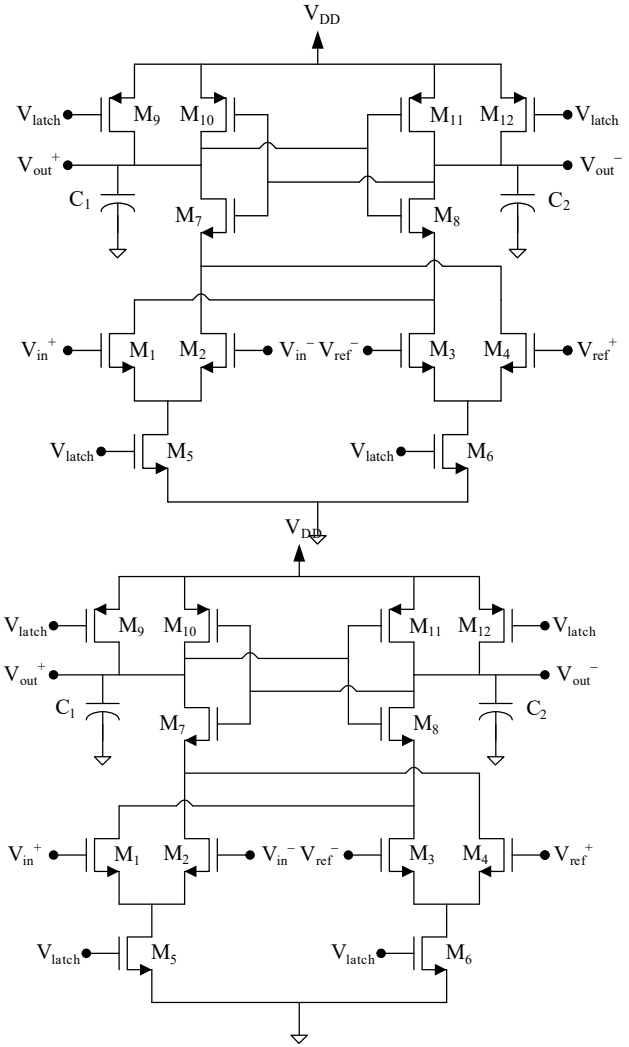


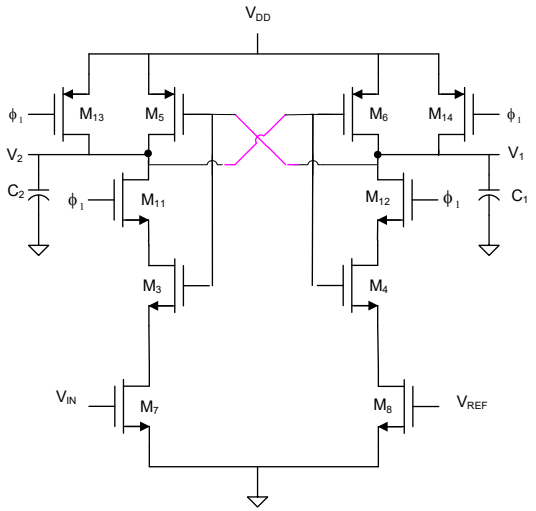
Single-Ended

- Mx used to reduce (eliminate) previous code dependence on comparator decision
- Regenerative feedback often used to force decision when differential inputs are small
- Several variants of clocked comparators are available
- Important to not have trip point dependent upon previous comparison results
- Often one or more linear gain stages precede the regenerative stage
- Power dissipation can be small in regenerative feedback comparators
- Large offset voltage (100mV or more) common for regenerative feedback comparators

Clocked Comparator with Regenerative Feedback







V_{REF} denotes V_{DACk} in these figures

Flash ADC Summary

Flash ADC

- Very fast
- Simple structure
- Usually Clocked
- Bubble Removal Important
- Seldom over 6 or 7 bits of resolution

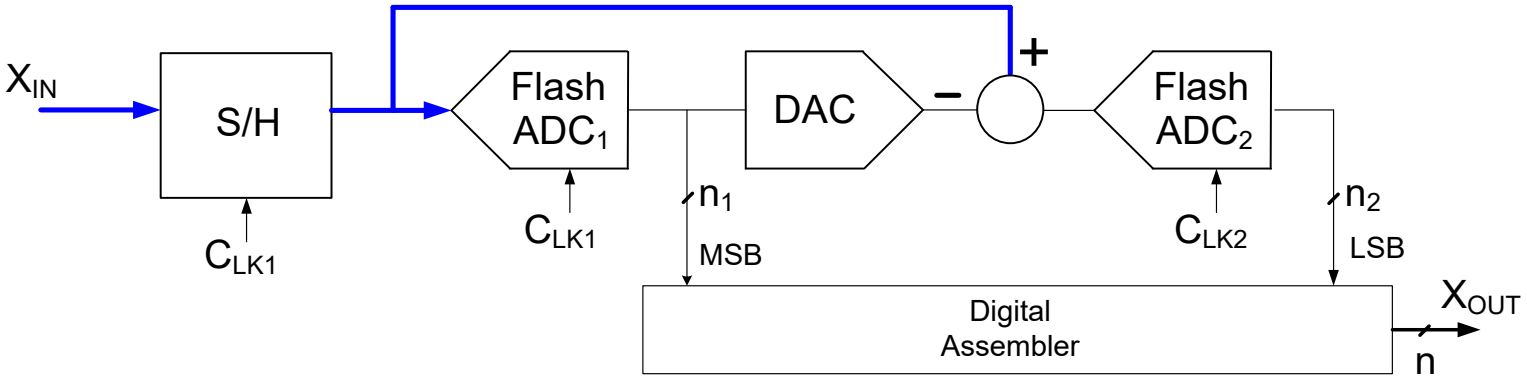
  - Flash ADC has some really desirable properties (simple and fast)
  - Wouldn't it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

Number of comparators increases geometrically --- 2^n

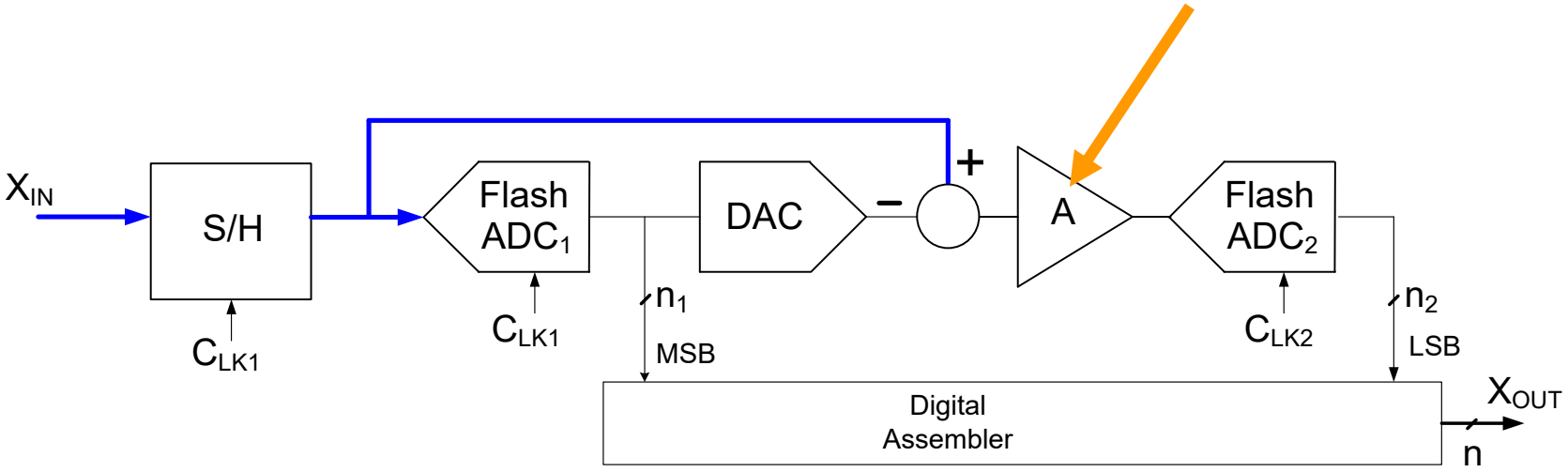
Two-Step Flash ADC



Can operate asynchronously (either after first S/H or even w/o S/H)

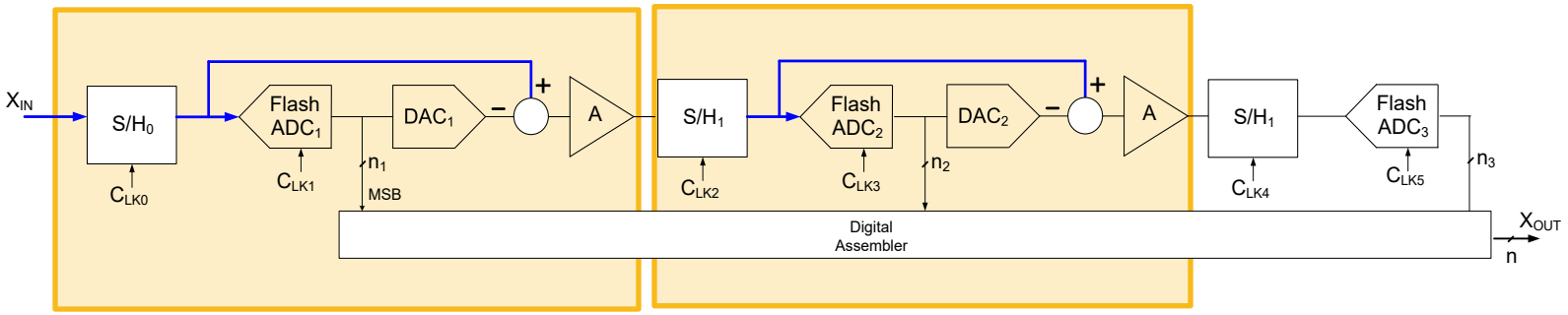
Reduces the number of comparators significantly
Reduces complexity of thermometer to binary converter
Residue signal at input to second Flash ADC is small
Difference block is a linear module that must be accurate
Have added a DAC that must have accuracy at the overall ADC resolution level
Speed of difference amplifier and DAC limit speed of ADC
Sequential clocking of ADC_1 and ADC_2 limits speed of ADC

Two-Step Flash ADC with Interstage Gain



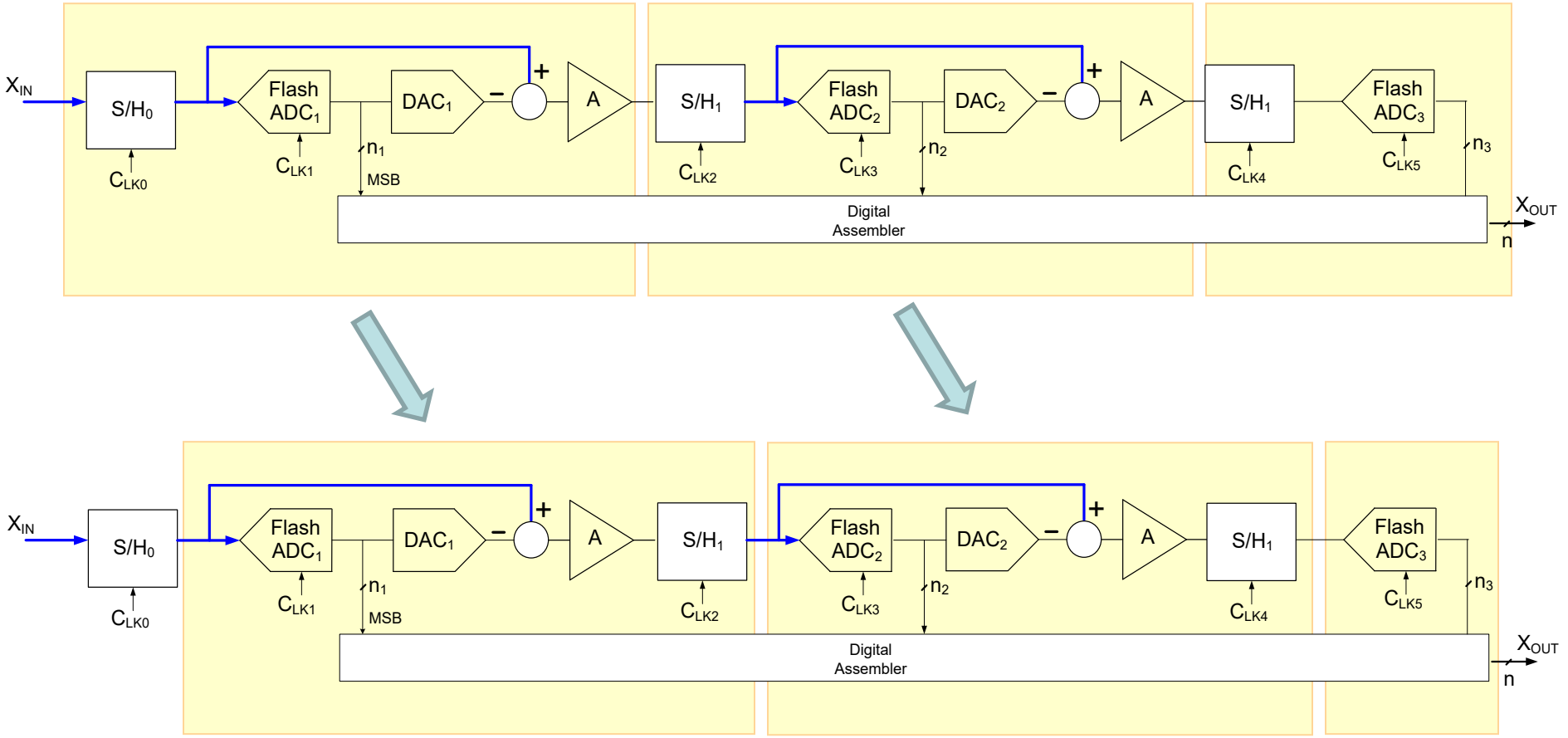
Increases level of signals into second Flash ADC (reducing offset concerns by a factor of A)
Speed of A of concern
Considerable power dissipation in A amplifier
Complexity is increasing significantly !

Three-Step Flash ADC with Interstage Gain and S/H



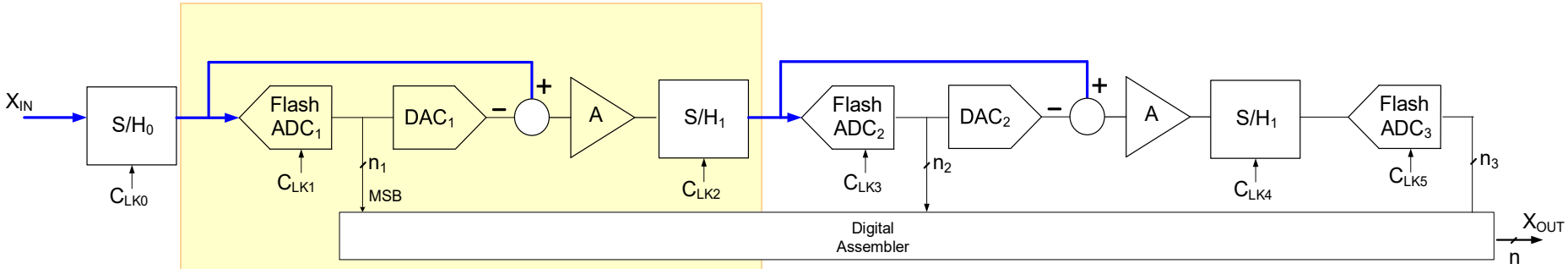
- Further reduces number of comparators needed!
- Even more complexity!
- But appears first two stages perform identical operations (if $n_1=n_2$)
- S/H$_1$ frees first stage to take another sample during second stage conversion
- S/H$_2$ frees second stage to take another sample during third stage conversion
- **This has a pipelining capability !**

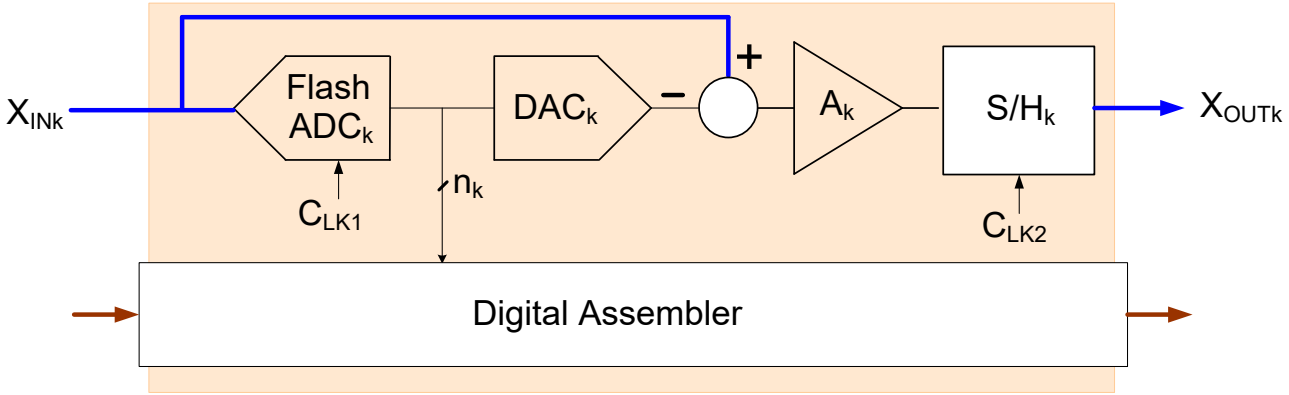
Three-Step Flash ADC with Interstage Gain and S/H



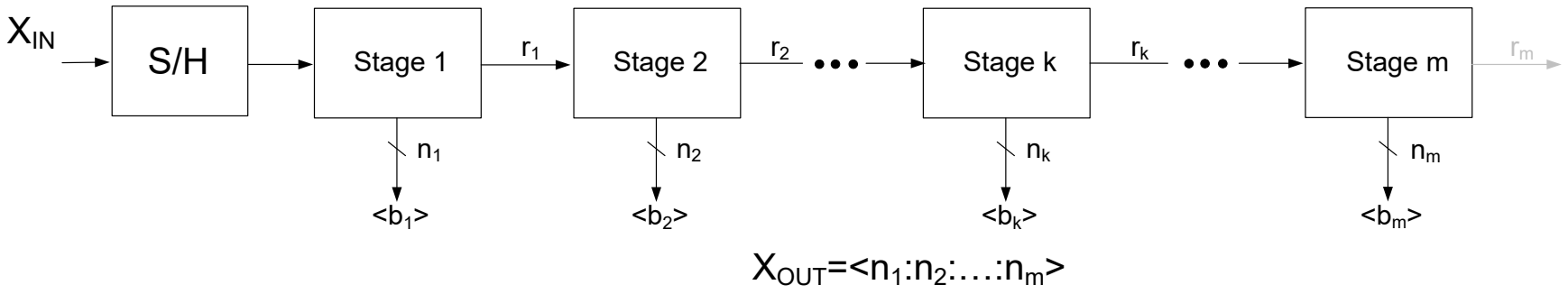
Same structure, different grouping!

Three-Step Flash ADC with Interstage Gain

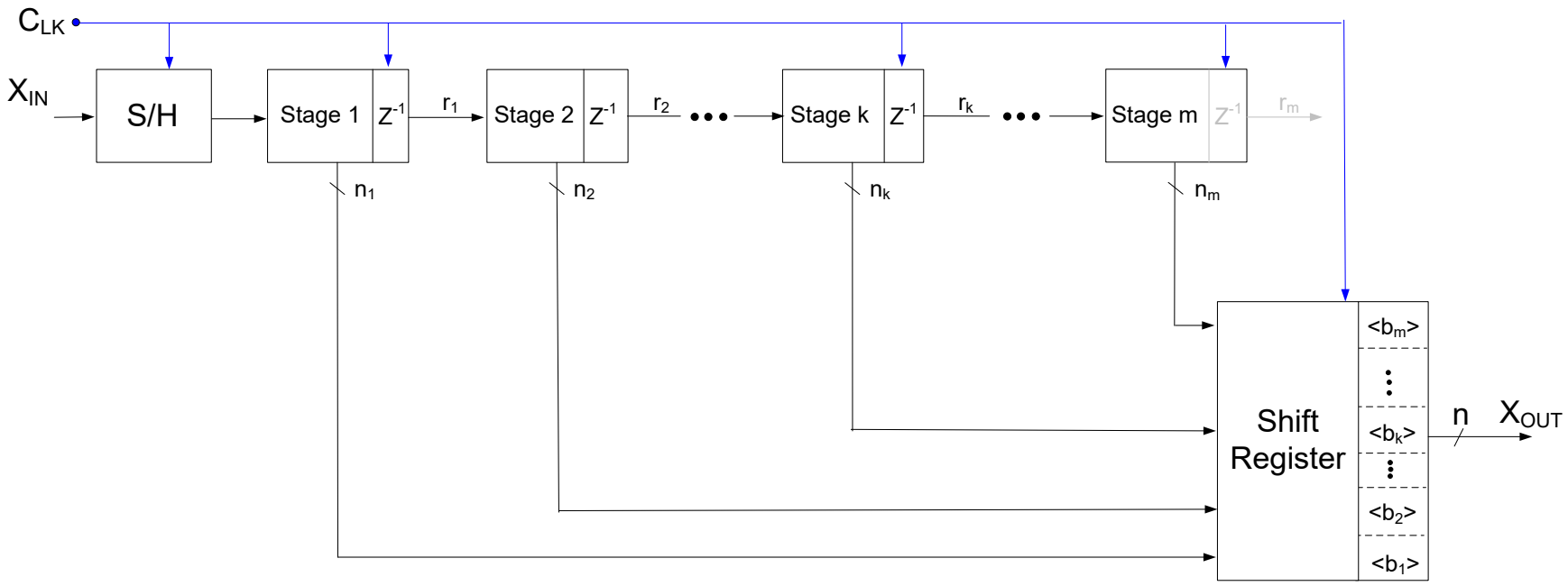




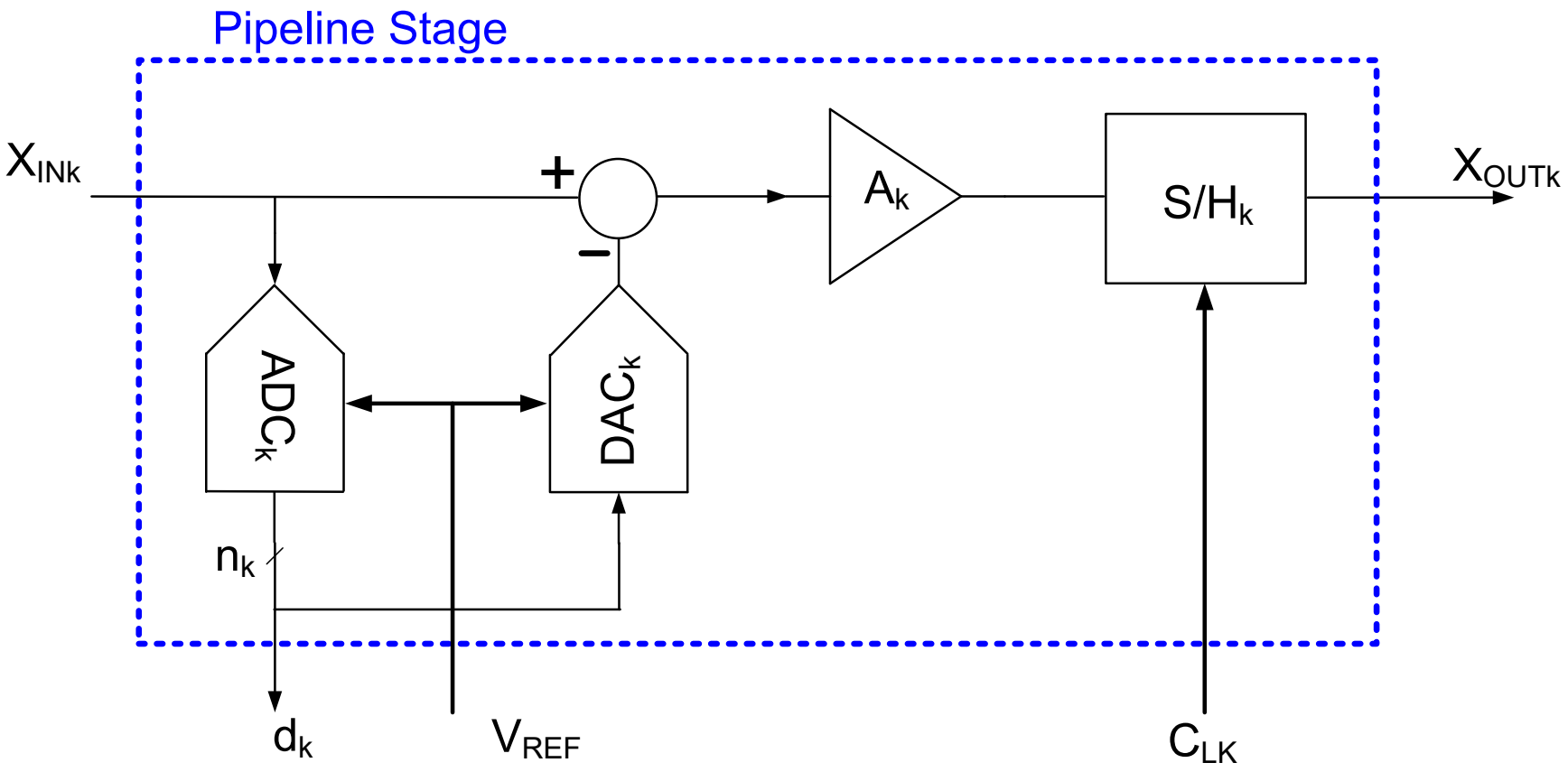
Pipelined ADC



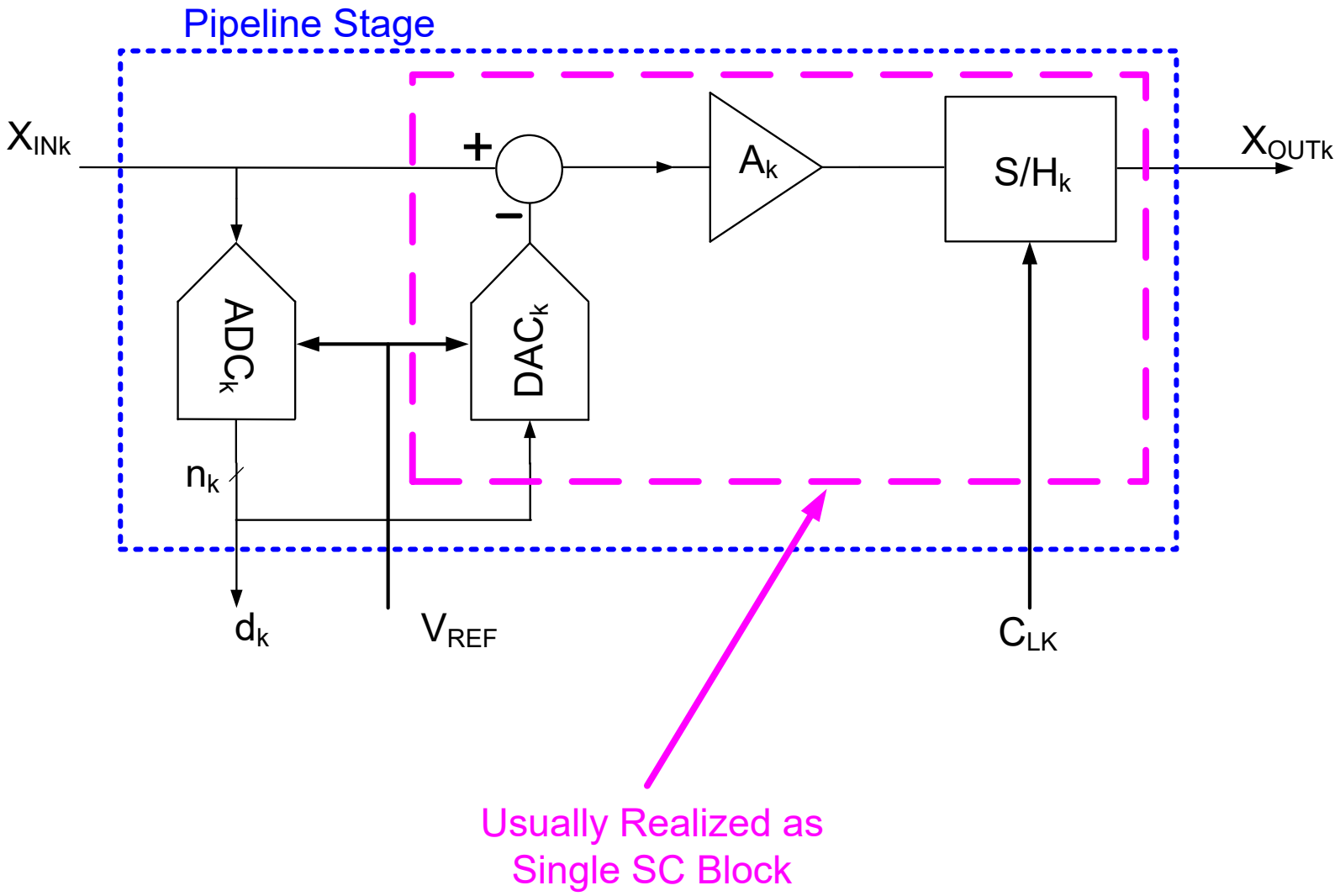
Pipelined ADC



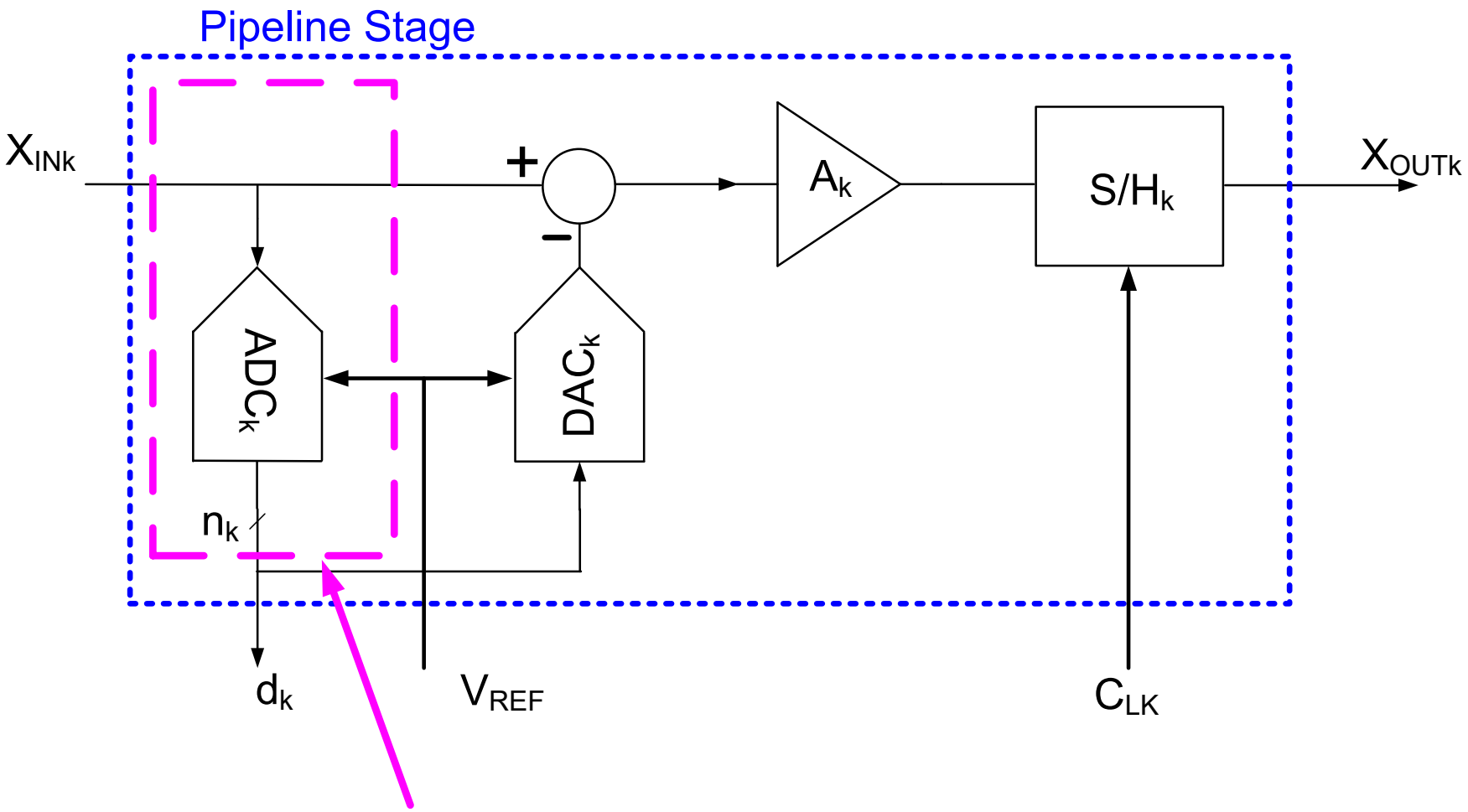
Pipelined ADC Stage k



Pipelined ADC Stage k

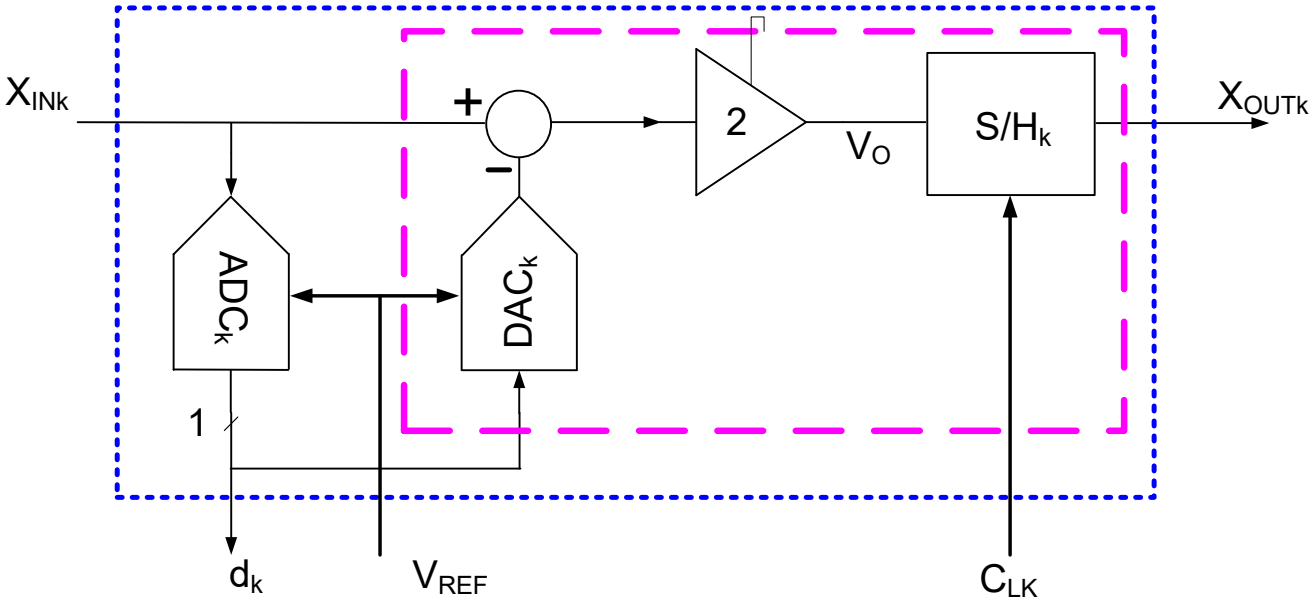


Pipelined ADC Stage k



Pipelined ADC Stage k

Pipeline Stage for 1 bit/stage

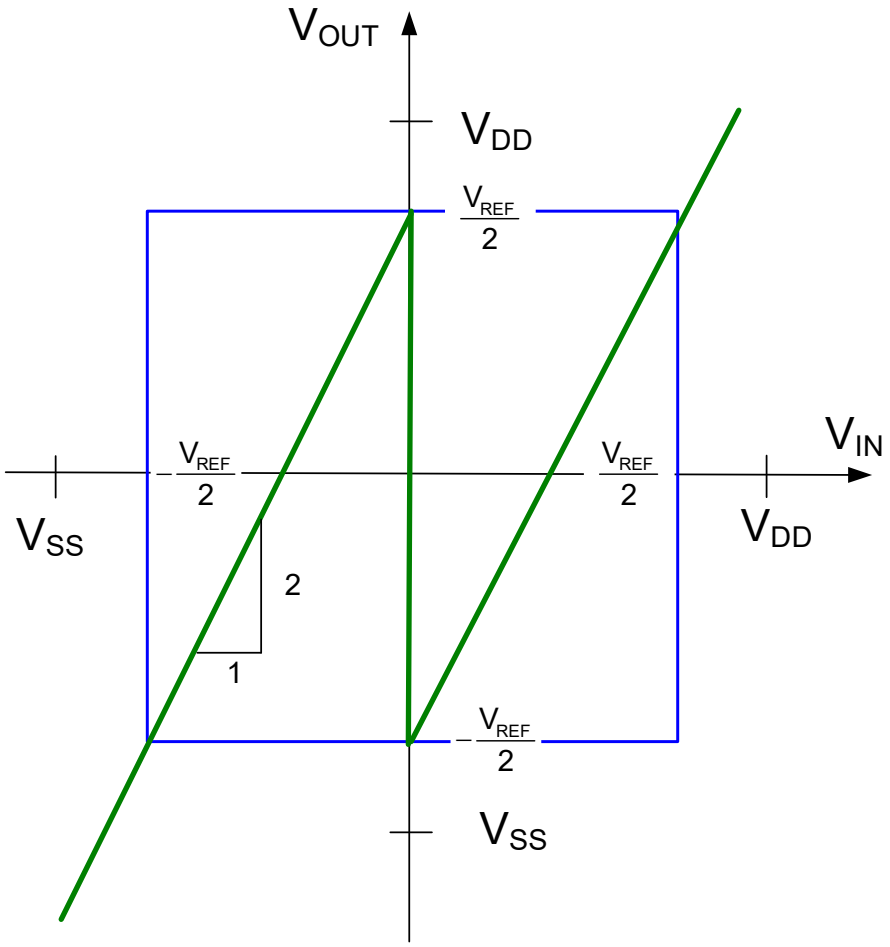


Assuming $-\frac{V_{REF}}{2} < V_{IN} < \frac{V_{REF}}{2}$

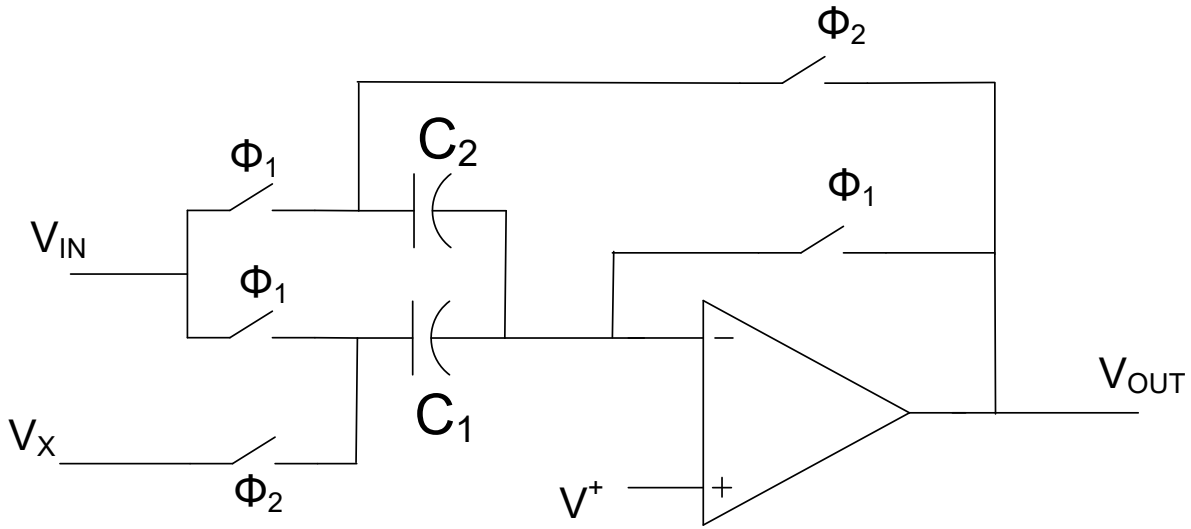
$$V_O = \begin{cases} 2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

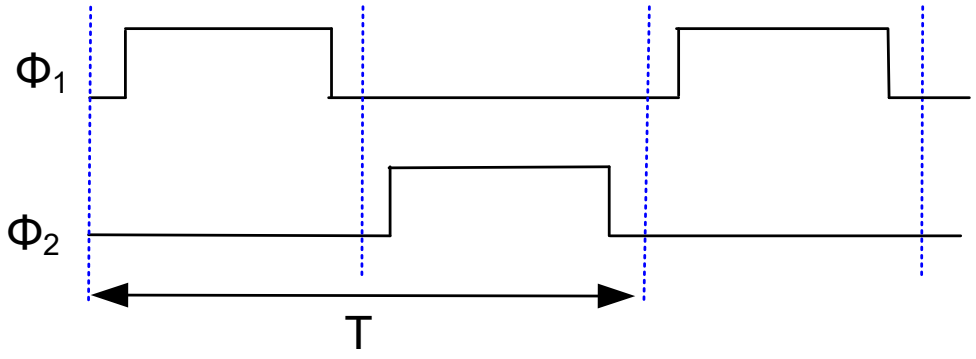
Transfer Characteristics for 1 bit/stage

$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$



Consider the following circuit





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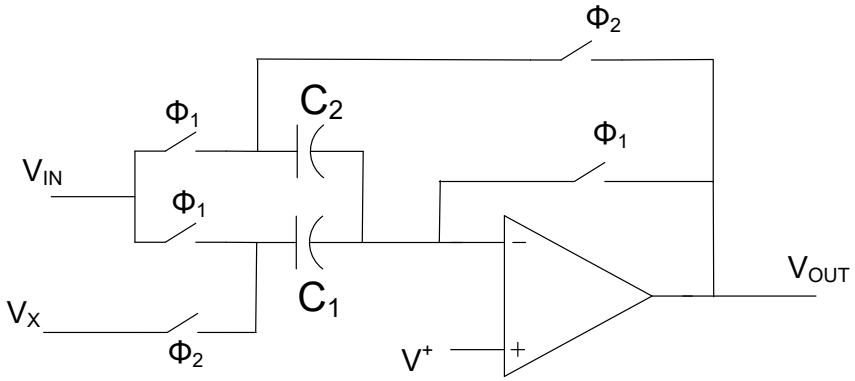
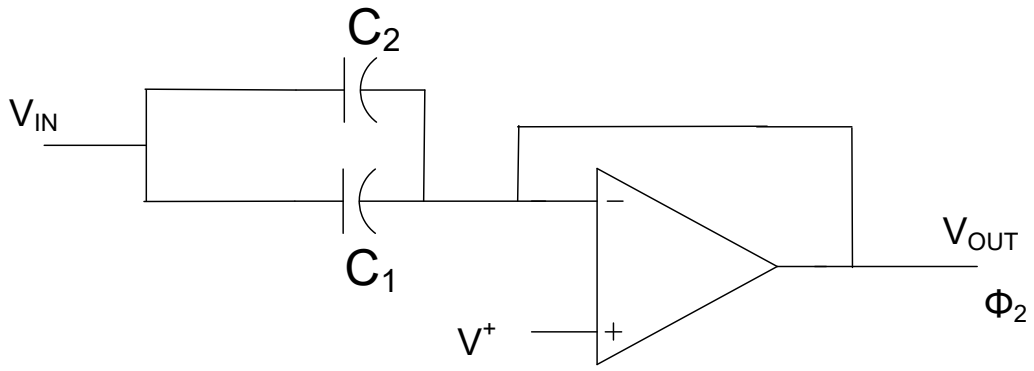
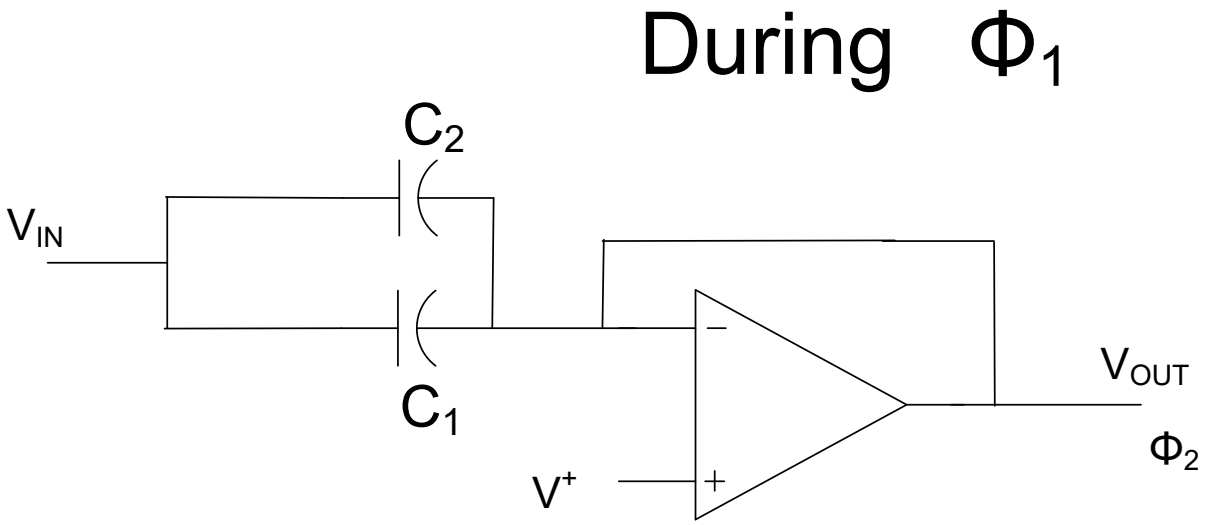


During Φ_1

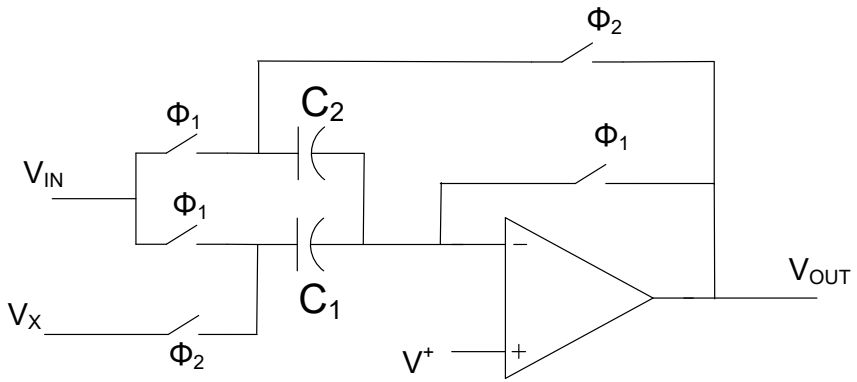


Consider the following circuit

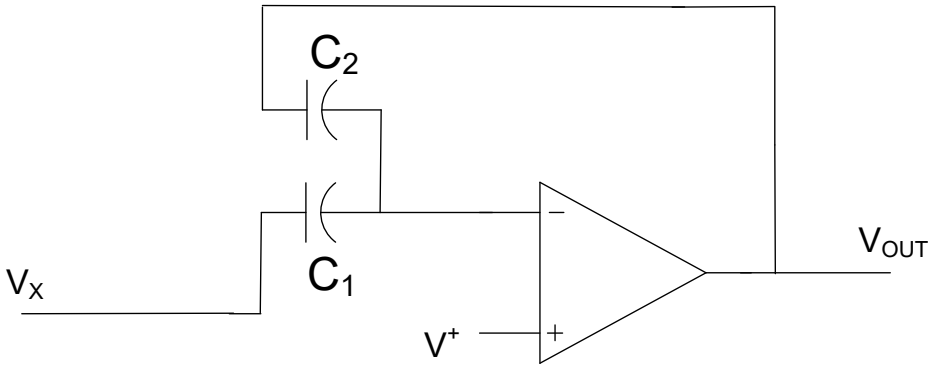


$$Q_1 = C_1\left(V_{IN} - V^+\right)$$
$$Q_2 = C_2\left(V_{IN} - V^+\right)$$

Consider the following circuit



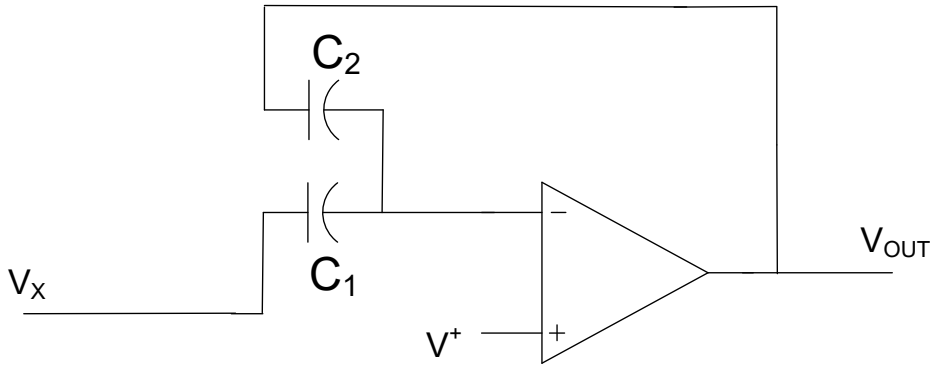
During Φ_2



Consider the following circuit

$$Q_1 = C_1\left(V_{IN} - V^+\right)$$
$$Q_2 = C_2\left(V_{IN} - V^+\right)$$

During Φ_2



Define Q_{1T} to be the charge transferred from C_1 during phase Φ_2

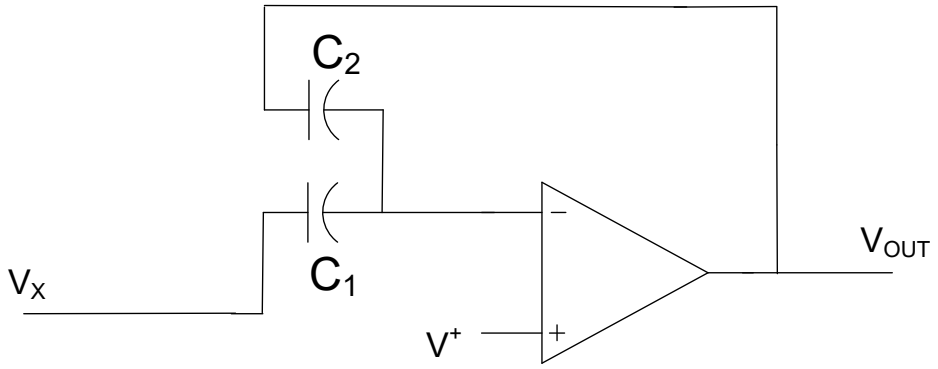
$$Q_{1T} = C_1\left(V_{IN} - V^+\right) - C_1\left(V_X - V^+\right) = C_1\left(V_{IN} - V_X\right)$$

Define Q_{2F} to be the total charge on C_2 during phase Φ_2

$$Q_{2F} = Q_2 + Q_{1T} = C_2\left(V_{IN} - V^+\right) + C_1\left(V_{IN} - V_X\right) = \left(C_1 + C_2\right)V_{IN} - C_2V^+ - C_1V_X$$

Consider the following circuit

During Φ_2

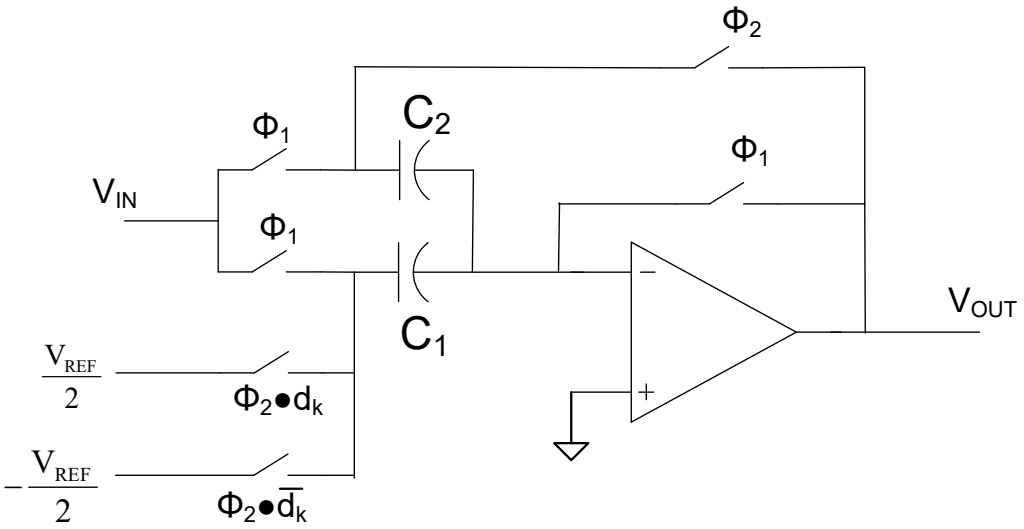


$$Q_{2F} = (C_1 + C_2)V_{IN} - C_2V^+ - C_1V_X$$

$$V_{C2F} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - V^+ - \frac{C_1}{C_2}V_X$$

$$V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X$$

Consider the following circuit

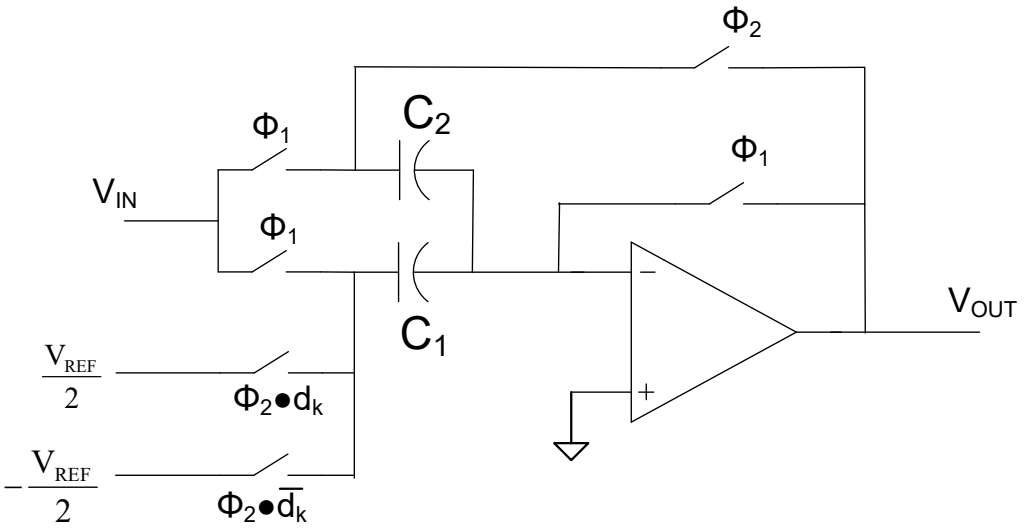


$$V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X$$

If $C_1 = C_2 = C$ and $V_X = -\frac{V_{REF}}{2}$

$$V_{OUTF} = 2V_{IN} + \frac{V_{REF}}{2}$$

Consider the following circuit



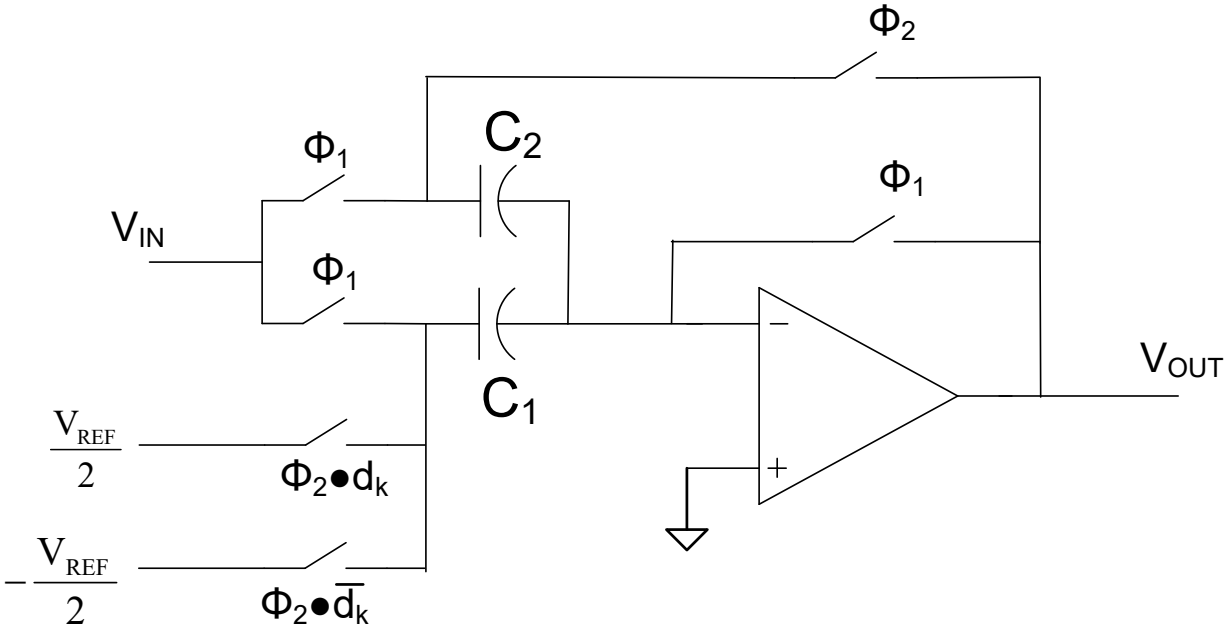
$$V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X$$

Likewise

If $C_1 = C_2 = C$ and $V_X = \frac{V_{REF}}{2}$

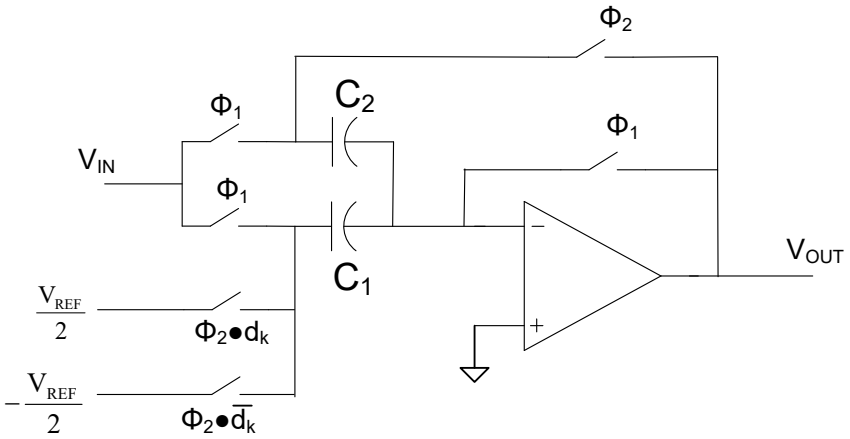
$$V_{OUTF} = 2V_{IN} - \frac{V_{REF}}{2}$$

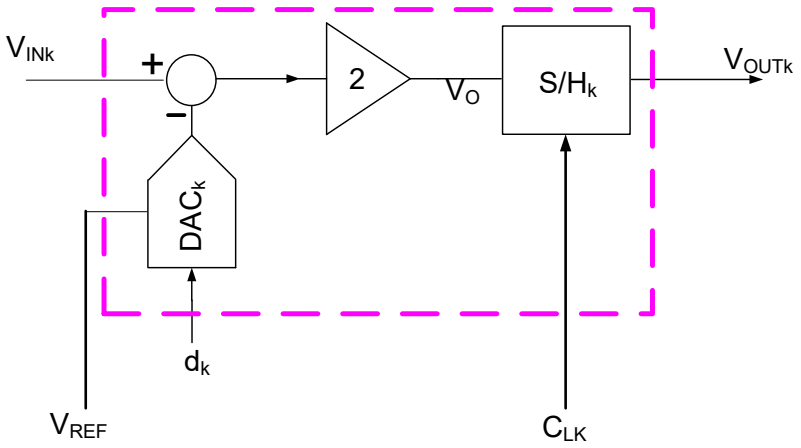
Observe



$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

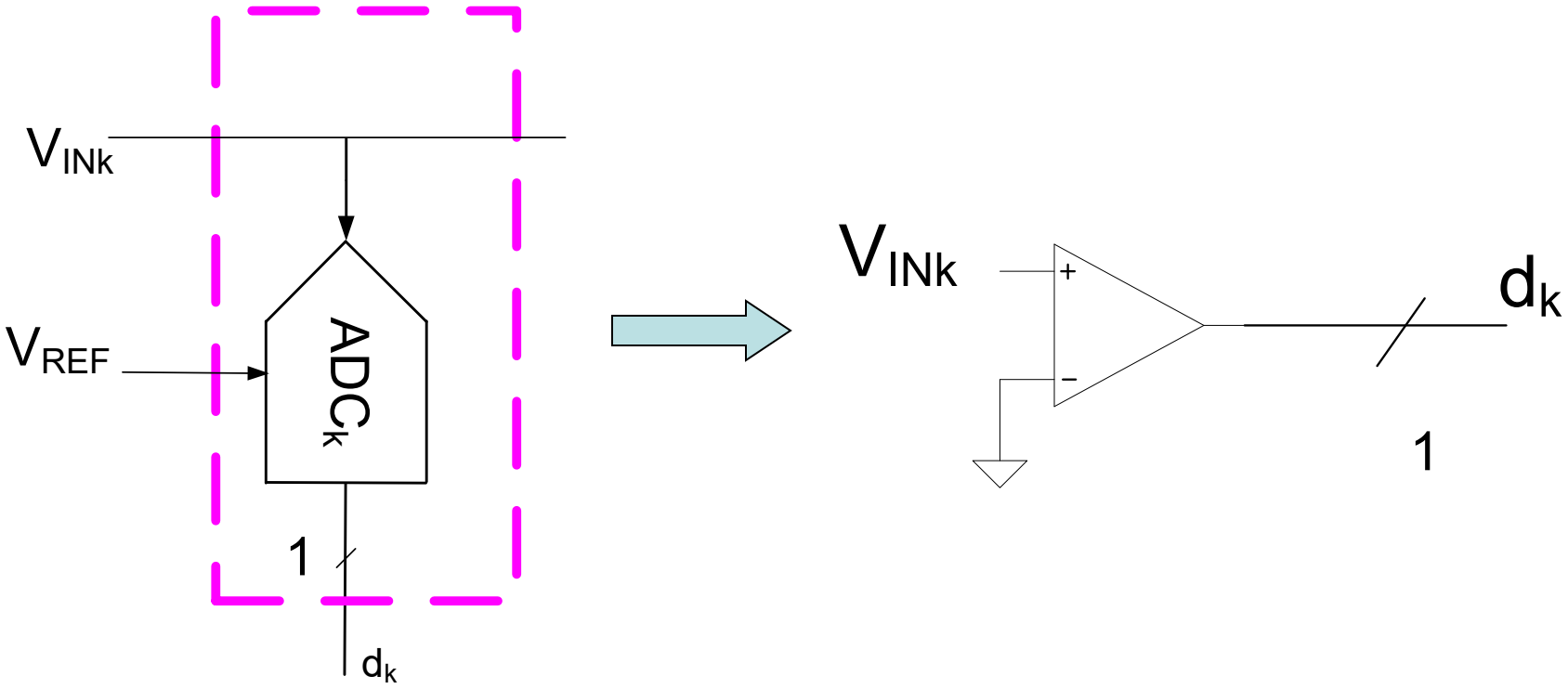
1-bit/Stage Pipeline Implementation



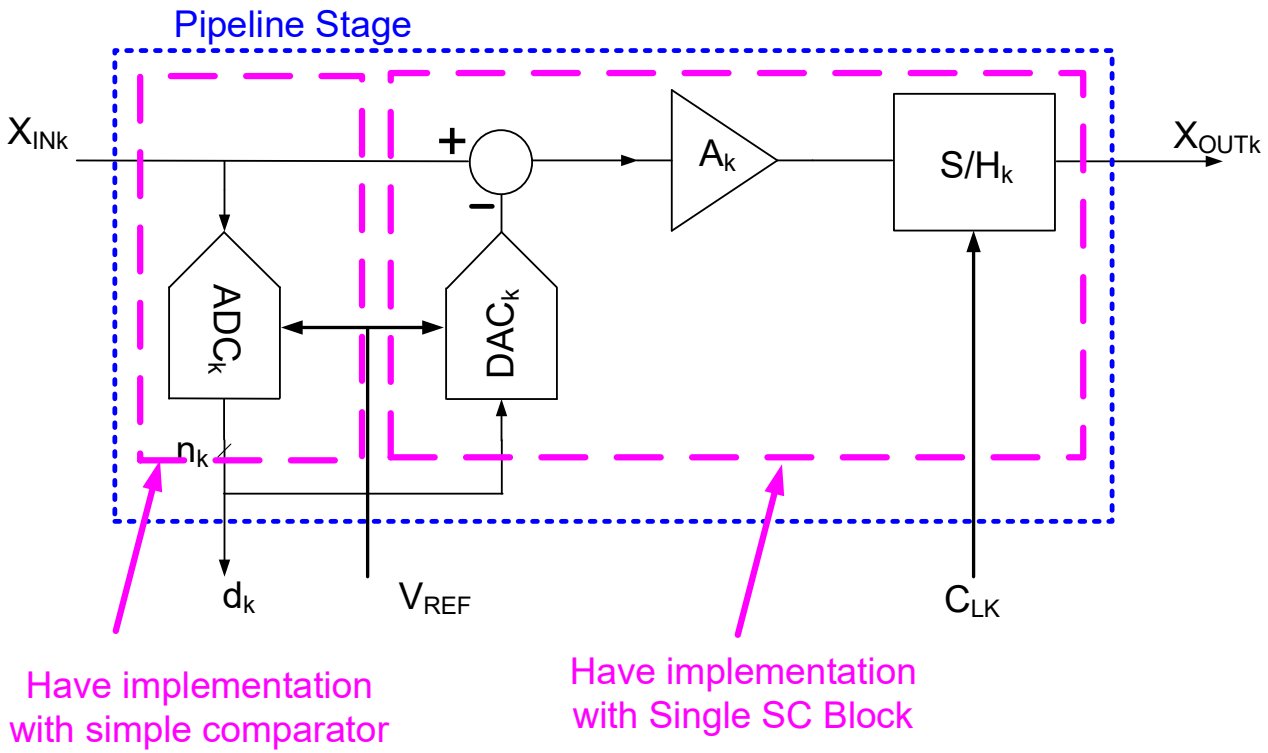


$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

1-bit/Stage Pipeline Implementation



Pipelined ADC Stage k

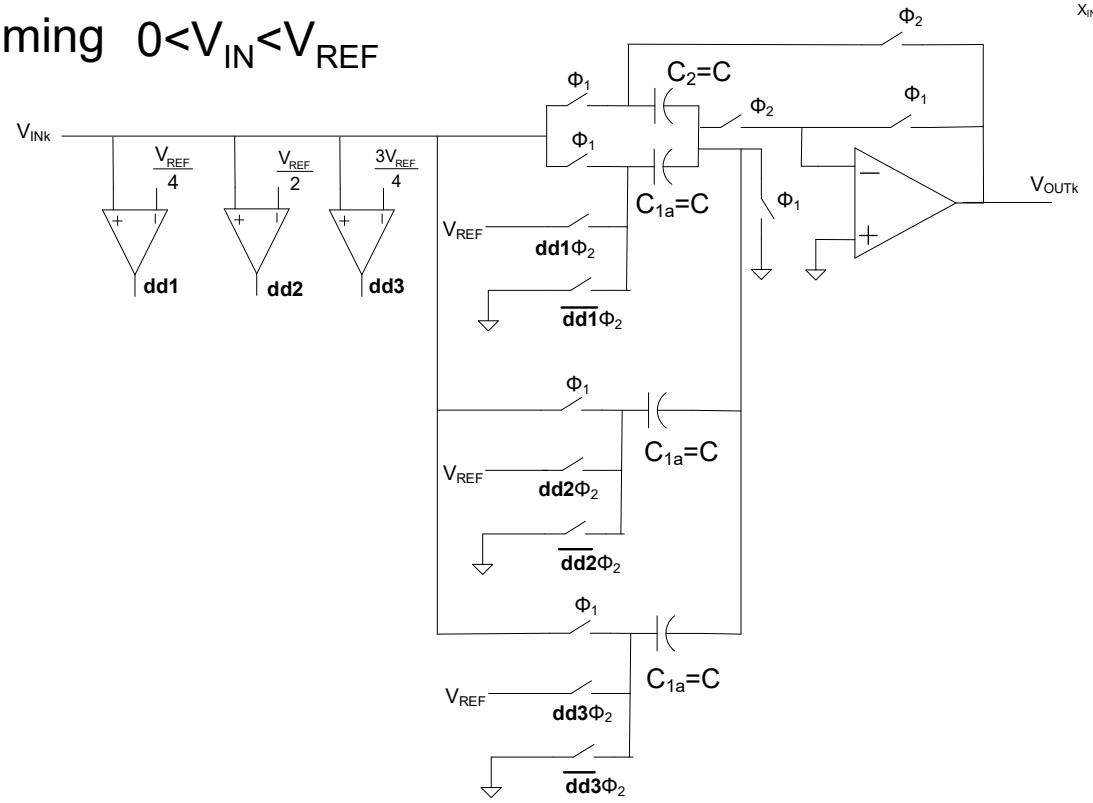


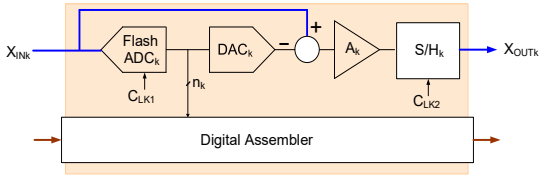
- Have shown simple implementation with 1-bit/stage structure
- Implementations with 2-bits/stage or 3-bits/stage also straightforward

Typical SC Pipeline Stage

For 2 bits/stage (Digital Assembler not shown)

Assuming $0<V_{IN}<V_{REF}$



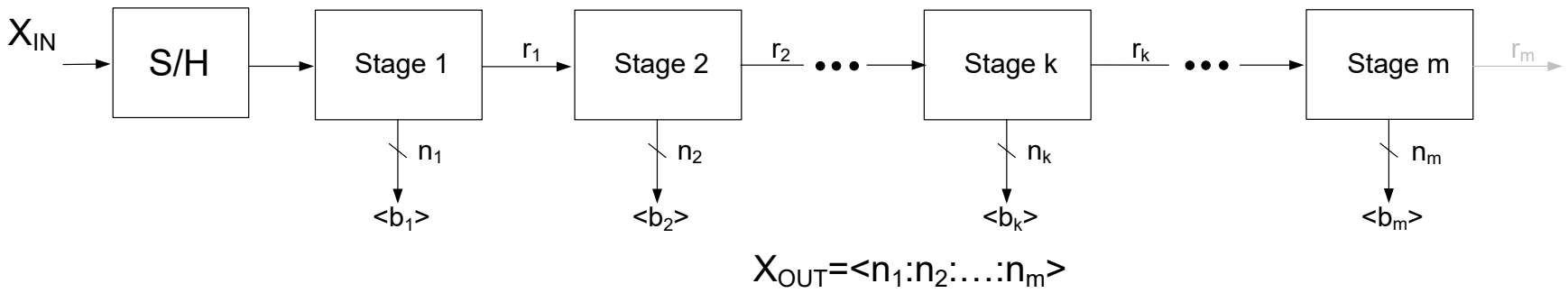


Gain =4

$$V_{OUT}=V_{IN}\left(1+\frac{C_{1a}+C_{1b}+C_{1c}}{C_2}\right)-\left(d_{d1}\left(\frac{C_{1a}}{C_2}\right)+d_{d2}\left(\frac{C_{1b}}{C_2}\right)+d_{d3}\left(\frac{C_{1c}}{C_2}\right)\right)V_{REF} \Rightarrow V_{OUTk}=4V_{INk}-\left(d_{dd1}+d_{dd2}+d_{dd3}\right)V_{REF}$$

- Directly use thermometer code outputs
- Can be extended to more bits/stage
- Accurate gain possible with good layout

Pipelined ADC



- Pipelined structure is widely used
- More than one bit/stage is often used
- Optimal number of bits/stage still an area of debate
- Conceptually can simply design one stage and then copy/paste to increase resolution
- Accuracy (and correspondingly power) in latter stages can be dramatically reduced
- Most power consumed in op amps
- Power dominantly allocated to S/H and MSB stages

Stay Safe and Stay Healthy !

End of Lecture 38